Press release

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Dipartimento di Fisica, Università di Perugia – I-06100 Perugia, Italy

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Computing with noise takes time

Can a computer still be operated in the presence of large fluctuations of the operating voltages?

According to a research just published in applied Physics Letters the presence of noise sets an upper limit to how fast (but also on how slow) a computer can work.

The present tendency to scale down computing devices has reached limits where ambient electrical noise becomes a serious threat to the correct functioning of such devices.

In a recent research conducted at the **Noise in Physical Systems** (**N.i.P.S**) **Laboratory** at the Physics Department of the University of Perugia, the role of noise in the functioning of basic logic gates has been studied with the aim of designing a new strategy toward the implementation of nanoscale computers. The research is part of a larger effort organized in the E.C. (European Commission) funded project, denominated SUBTLE: Sub KT Transistors and Sensors (FPVI STREP Contract No. 034236).

That noise could affect the performances of computing devices is not something new or unexpected. In modern transistor-based logic gates, the impact of noise has become even more relevant since the voltage scaling strategy aimed at decreasing the dissipated power has increased the probability of error due to the reduced switching threshold voltage levels.

Prof. Luca Gammaitoni from N.i.P.S Laboratory has demonstrated that the presence of a generic noise interferes with the switching mechanism of basic logic gates in order to introduce an additional delay to the standard “propagation delay” that affect the device functioning and is related to the physics of the device. Such an additional delay is a function of the noise statistics and becomes significant in the presence of noise of intensity comparable with the difference between the input signal amplitude and the threshold value. In these conditions the noise-induced delay can seriously limit the computing speed of standard logic gates.

More specifically, the research in the N.i.P.S Laboratory demonstrated that computation in threshold-based devices e.g., transistor-based logic gates, can still be performed provided that the system clock is operated according to the existence of a proper idle time-interval that is a function of the noise properties. In fact there are two concomitant effects that affect the functioning of the switch mechanism: 1) the noise can initially prevent the input signal from crossing the relevant threshold, postponing in time this event and thus resulting in a longer propagation delay (delayed switching error due to trapping). 2) Once the device switching is completed, the noise might cause a re-crossing of the opposite threshold causing a bit-flip error.

The role of noise in computing devices however can also be seen from a different perspective. Instead of being a mere disturbance it can be considered as an essential part in the computing process itself. This is the case for example, of the sub-threshold gate driving, i.e. when the driving signal is lower than the switching threshold. In the absence of noise no switch is possible and the gate cannot operate. Instead also a noise of small intensity can bring (in due time) the input signal above the threshold and thus drive the gate for the computing task. Scenarios where the noise can play a beneficial role are not new in the literature; see e.g. the *Stochastic Resonance* phenomenon or the *Dithering effect*. L. Gammaitoni addresses this case too, showing that, similarly to the over-threshold driving, it exists a proper time interval (idle time) where the error probability stays below a certain fixed value.

These results are potentially relevant in the design of nanoscale computers where thermal and ambient noises, instead of being a mere source of disturbances, could be useful components of the computing process. The phenomenology discussed in this paper is not related to a specific noise source, typical of a specific material, but can be observed in the presence of a wide variety of different noises, including thermal fluctuations of the gate mechanisms, Johnson noise in the carrier conduction, shot noise in the ballistic transport, to mention few of the most common. Evidences of the trapping phenomena in GaSa/AlGaAs-based electron Y-branch switches in the presence of internal noise have been observed.

In summary, this work demonstrates that the careful consideration of the noise effects, together with a proper choice of the "idle time interval" lead to a prescription for the minimization of the error probability that can be summarized as follows:

In a noisy environment you can still compute by using the usual threshold-crossing logic gates, provided that you wait long enough, but not too long.

References:

- *Noise limited computational speed*, L. Gammaitoni, Appl. Phys. Lett. 91, 224104 (2007)
- web site of the SUBTLE Project: subtle.fisica.unipg.it

NiPS Laboratory press office

www.nipslab.org

T. +390755852733

e-mail comunicazione@nipslab.org