Semiconductor Nanowire Simulation for Technology Design

Tyndall National Institute
Institiúid Náisiúnta

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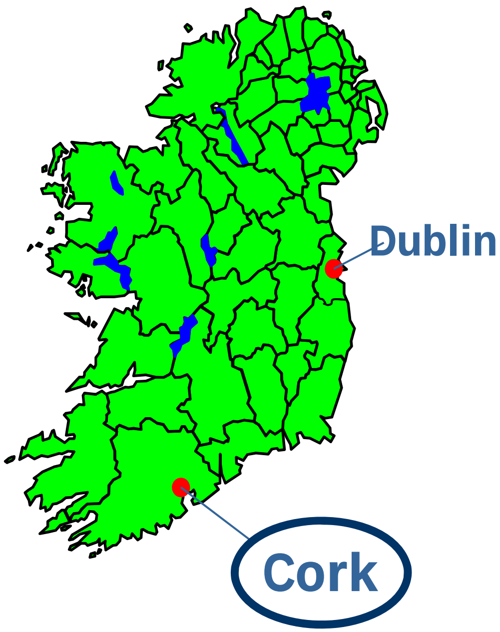


Tyndall National Institute

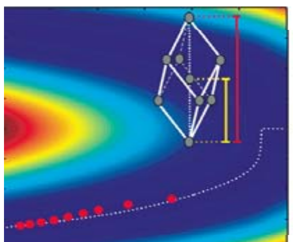
John Tyndall
1820 - 1893

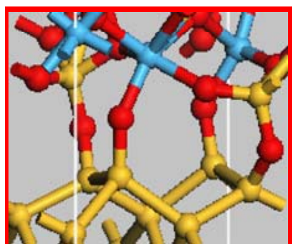
- Established in 2004 (NMRC, UCC, CIT)
  - largest research institute in Ireland
  - capital investment >€200M and annual income ~ €35M
  - 400 research engineers, scientists, students, interns & support staff
- Brings together researchers in:
  - Nanomaterials & Nanotechnology
  - Energy
  - Electronics
  - Photonics
  - Theory & Modelling
- Objectives:
  - Research into Information and Communication Technologies of strategic value to Ireland
  - Technology transfer and collaboration with industry
  - Education & training; Outreach to community

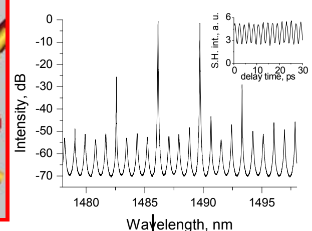
Theory, Modelling & Design Centre

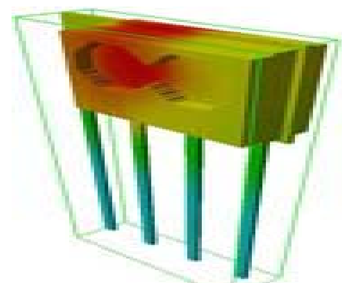
Combination of skills in physics, chemistry, materials science, engineering

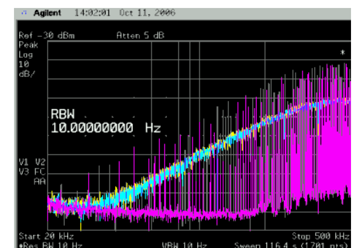
"from atoms to systems"









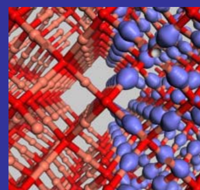


Basic Phenomena → Materials → Devices → Integration → Systems

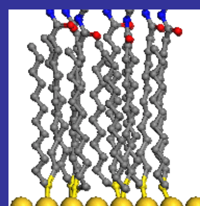
Condensed Matter | **Electronics Theory** | Photonics Theory | Circuits & Systems

Electronics Theory Group overview

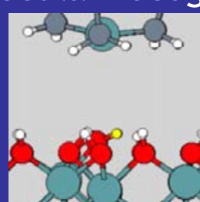
Materials



Oxide materials

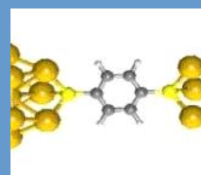


Self assembly and molecular recognition

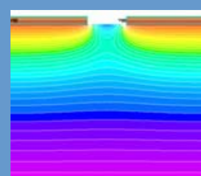


Processing and growth

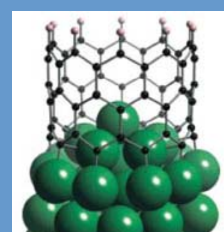
Devices



Molecular electronics

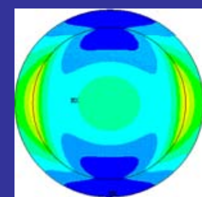


Low dimensional structures

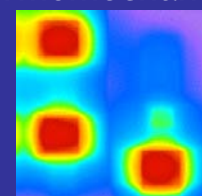


Nanoscience

Systems

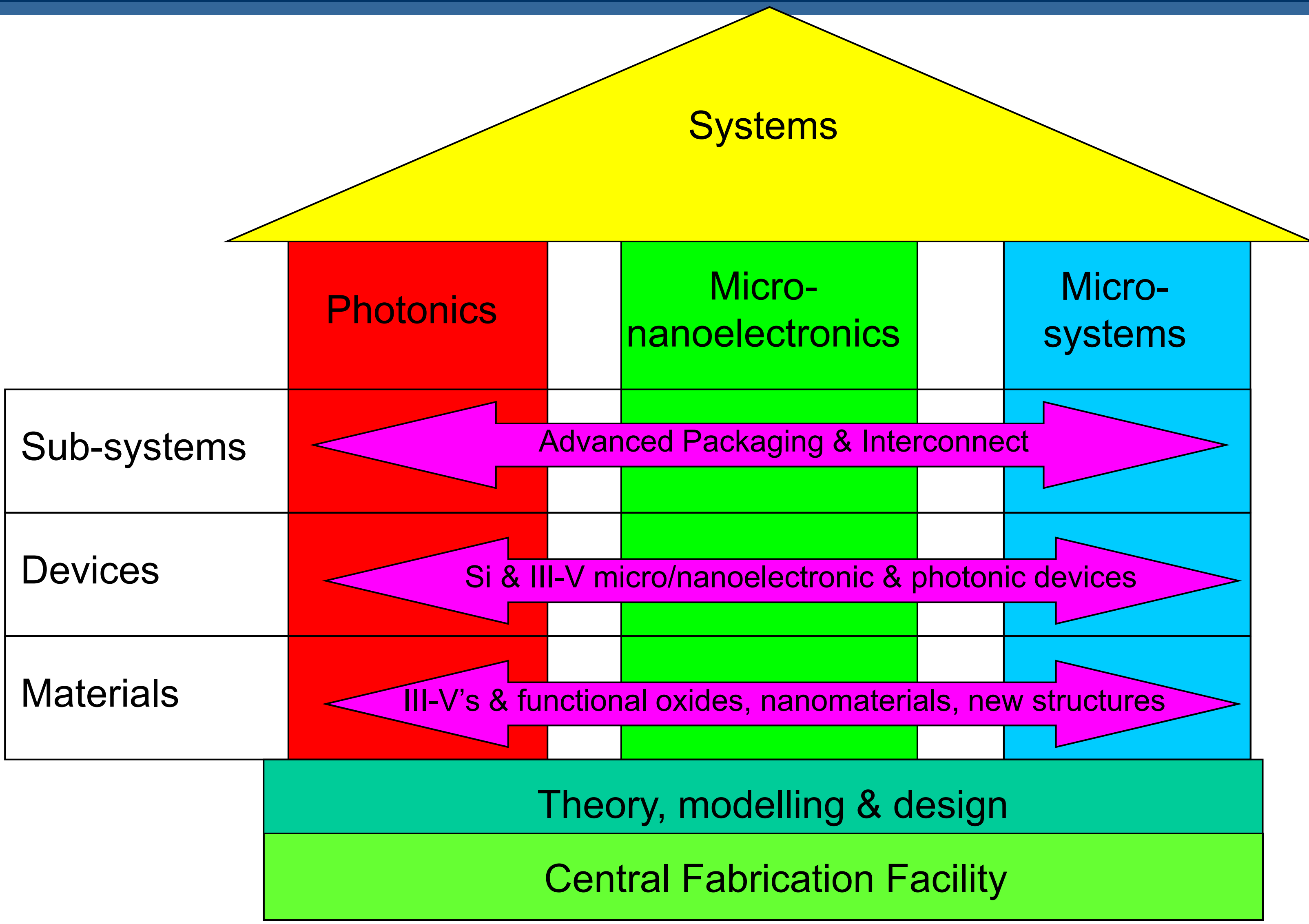


Thermomechanical

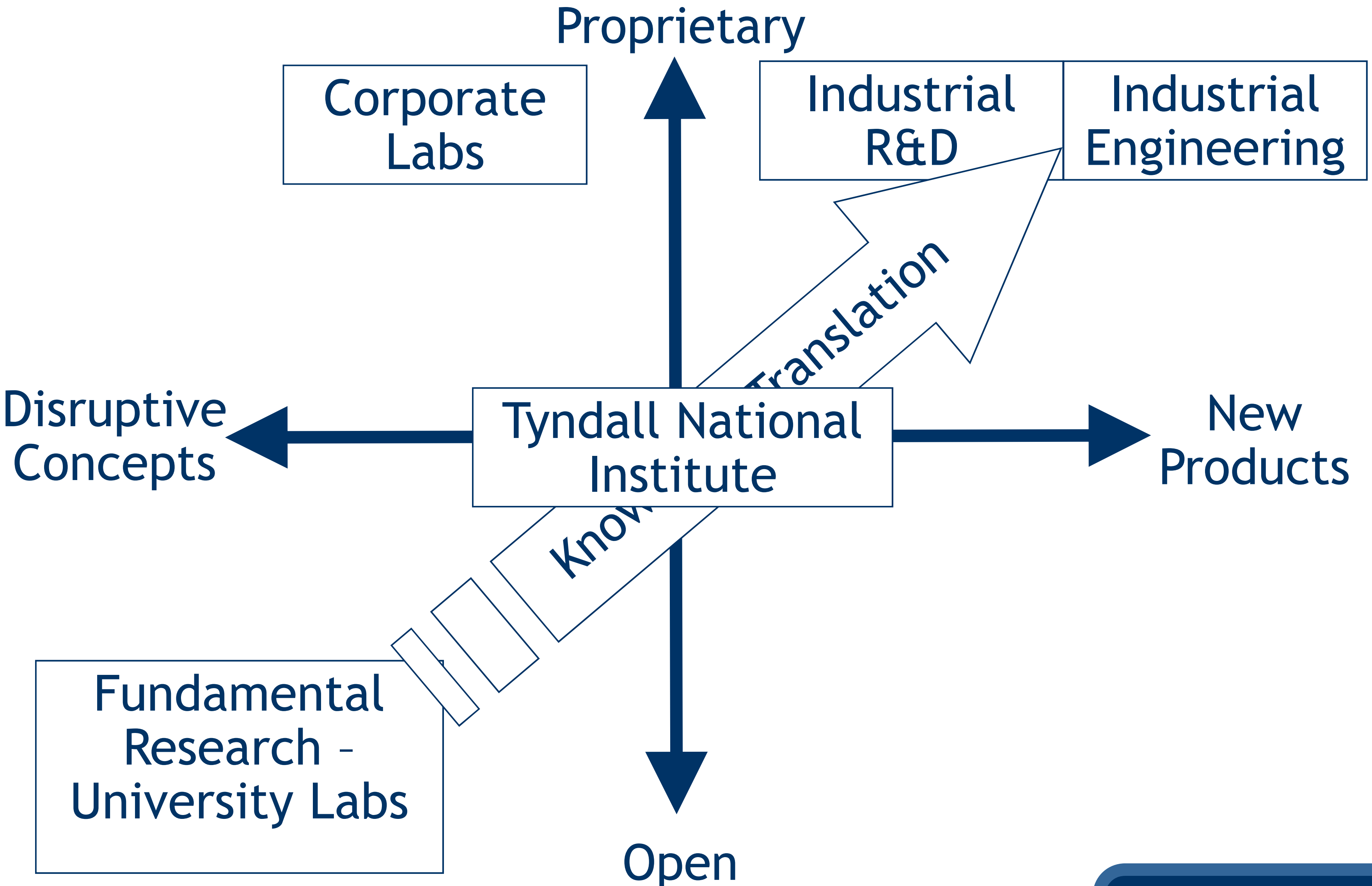


Thermal modelling

Technologies at Tyndall



Tyndall's Role



Overview

Motivation and aims:

Methodology

- Electronic structure
- Charge transport

Results

- Surface modification
- Charge transport in locally oxidised NWs
- Computational method development
- Electron-phonon coupling
- Nanowire-based CMOS

Concluding Remarks

Motivation and aims

Methodology

Results

Concluding Remarks

ZER0POWER

The International Energy Agency predicts:

- ICT and consumer electronics account for approximately 15% of global residential electricity consumption
- By 2030, energy use by household ICT and consumer electronics will triple consuming 1700TWh

“Building the nano-to-micro bridge

for

energy-sustainable ICT”

NiPS Laboratory
Noise in Physical Systems

UAB
Universitat Autònoma de Barcelona

University of Glasgow

Tyndall
National Institute

Why Zero-Power ICT?

Energy efficient ICT

- Low(er)-power devices for processing, sensing, communicating
- Energy dissipation & power management
- Renewable sources for consumer electronics and autonomous nano-scale devices

ICT for energy efficiency

- More efficient use of natural resources/energy by design
- Change of energy consumption patterns
- Direct gains by intelligent distributed sensing, for health, safety-critical systems, environmental monitoring, industrial management and control

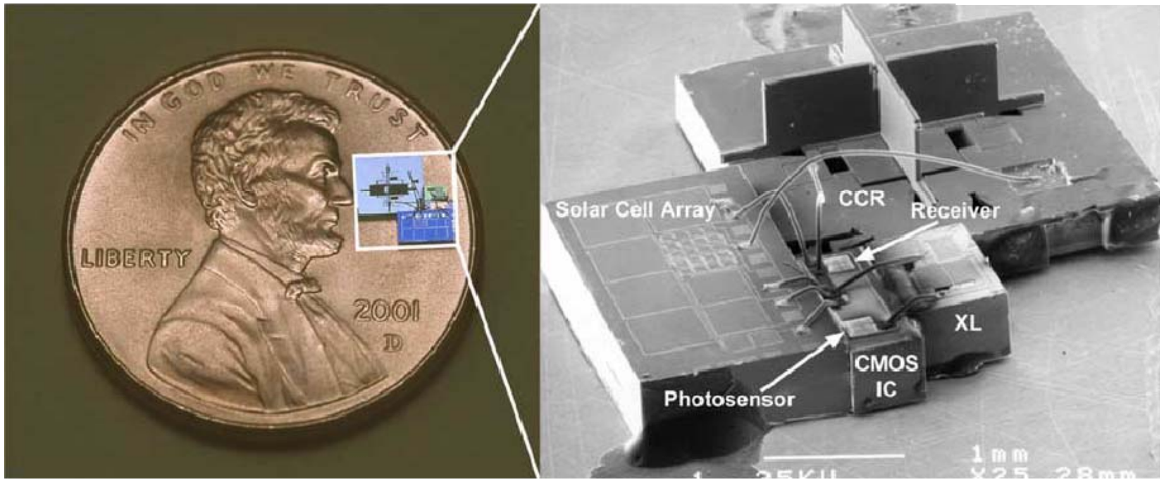
Smart Dust project
the Mica mote

"autonomous sensing, computing, and communication system packed into a cubic-millimeter mote to form the basis of integrated, massively distributed sensor networks"

B. Warneke, M. Last, B. Liebowitz, and K. S. J. Pister, Computer **34**, 44 (2001)

Off-the-self components

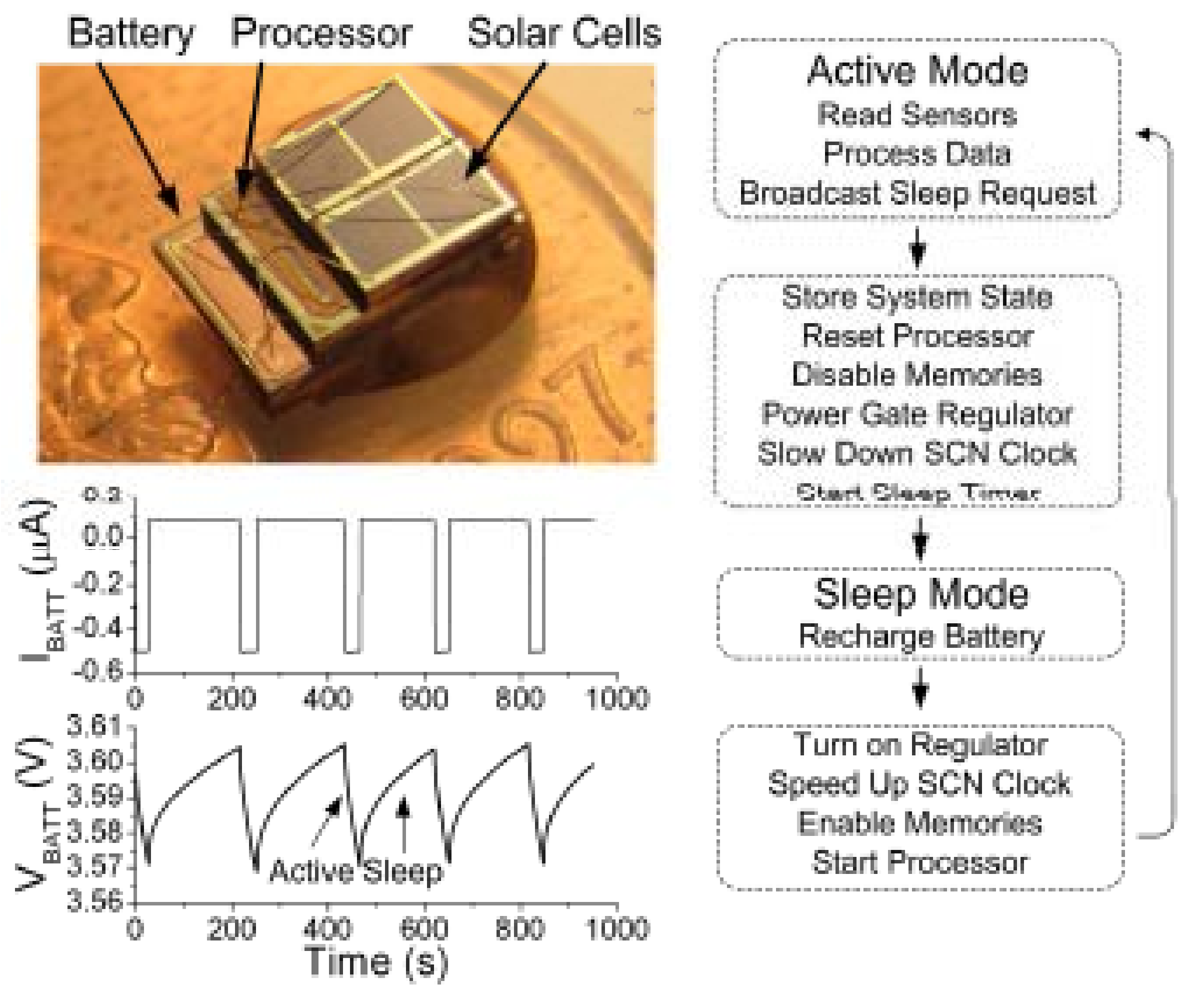
Custom solar cell, custom CMOS
→ 16mm^3



B.W. Cook and K. S. J. Pister, IEEE Proc. **94**, 1177 (2006)

Towards one cubic millimetre

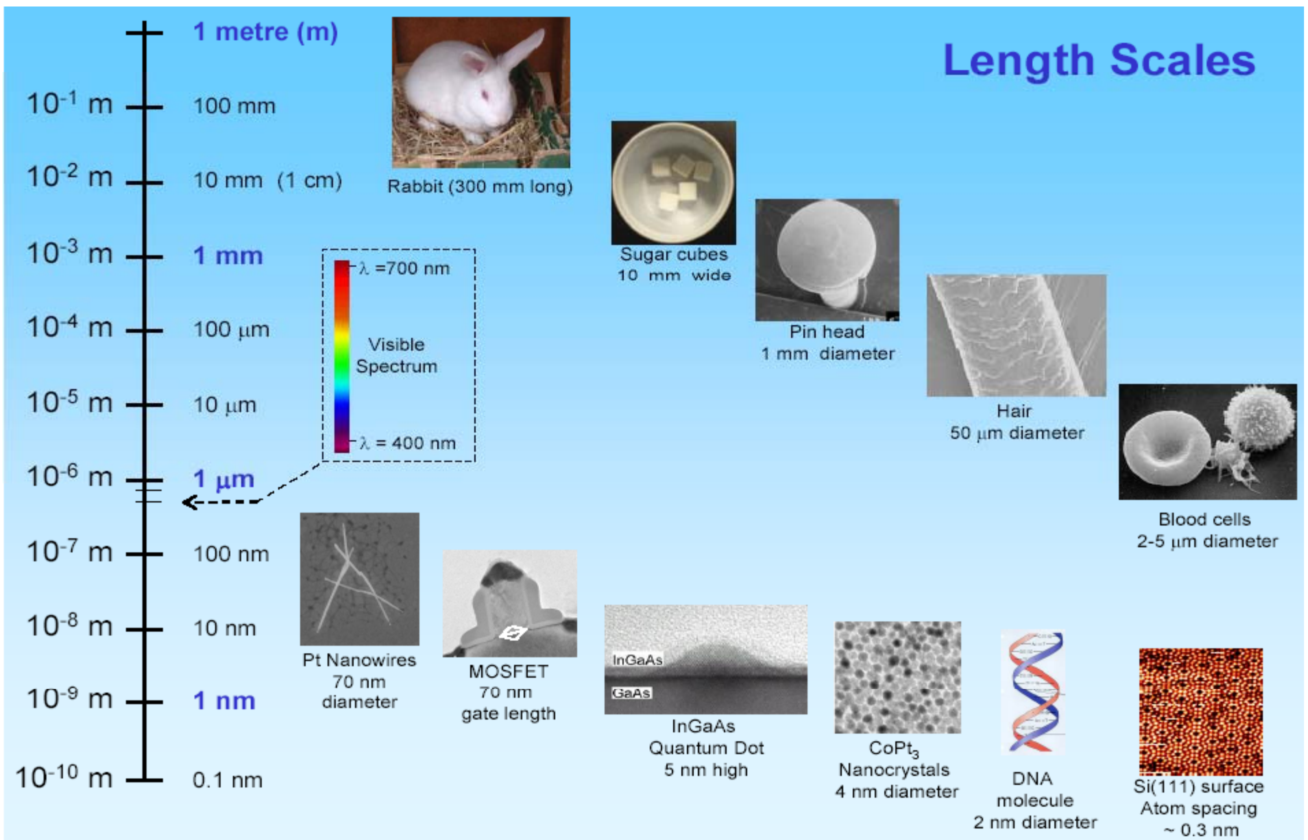
- ✓ Low-power active and sleep mode
- ✓ Thin-film Li battery
- ✓ Custom solar cells ~ 1mm^2
- ✓ Temperature & pressure sensor



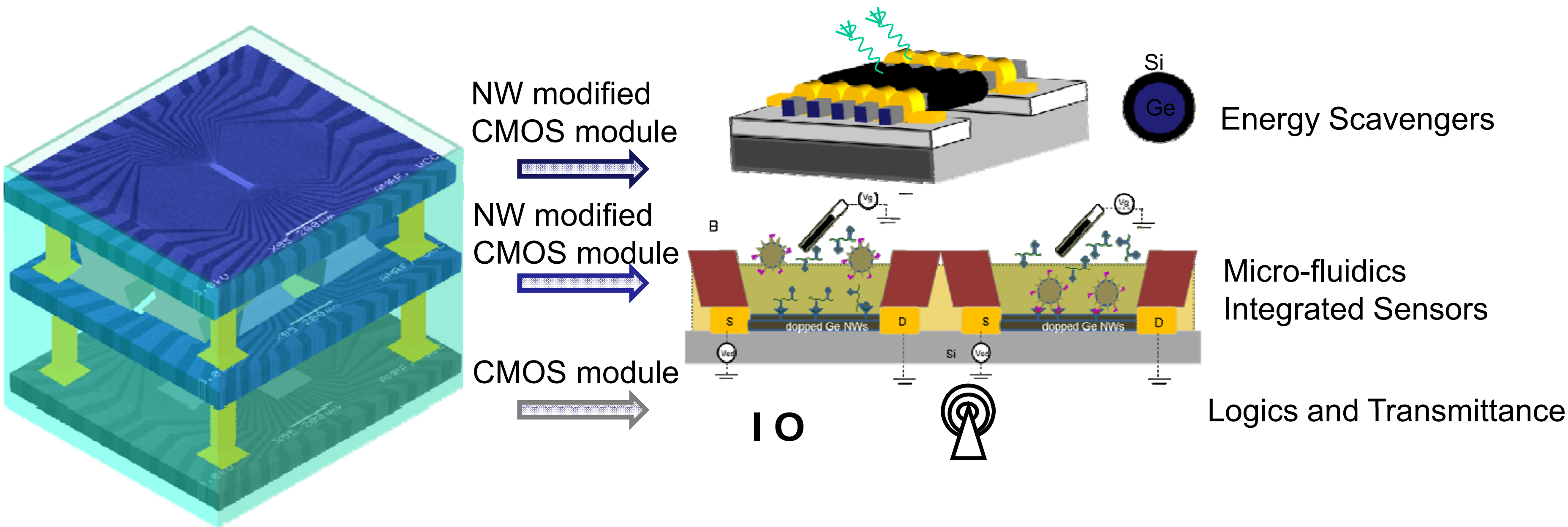
Blaauw group, Michigan

Definition (Wikipedia)

A nanowire is a nanostructure, with the diameter of the order of a nanometer. Alternatively, nanowires can be defined as structures that have a thickness or diameter constrained to tens of nanometers or less and an unconstrained length.



SiNAPS mote concept (see www.sinaps-fet.eu)



Energy harvesting possibilities

Battery operated systems

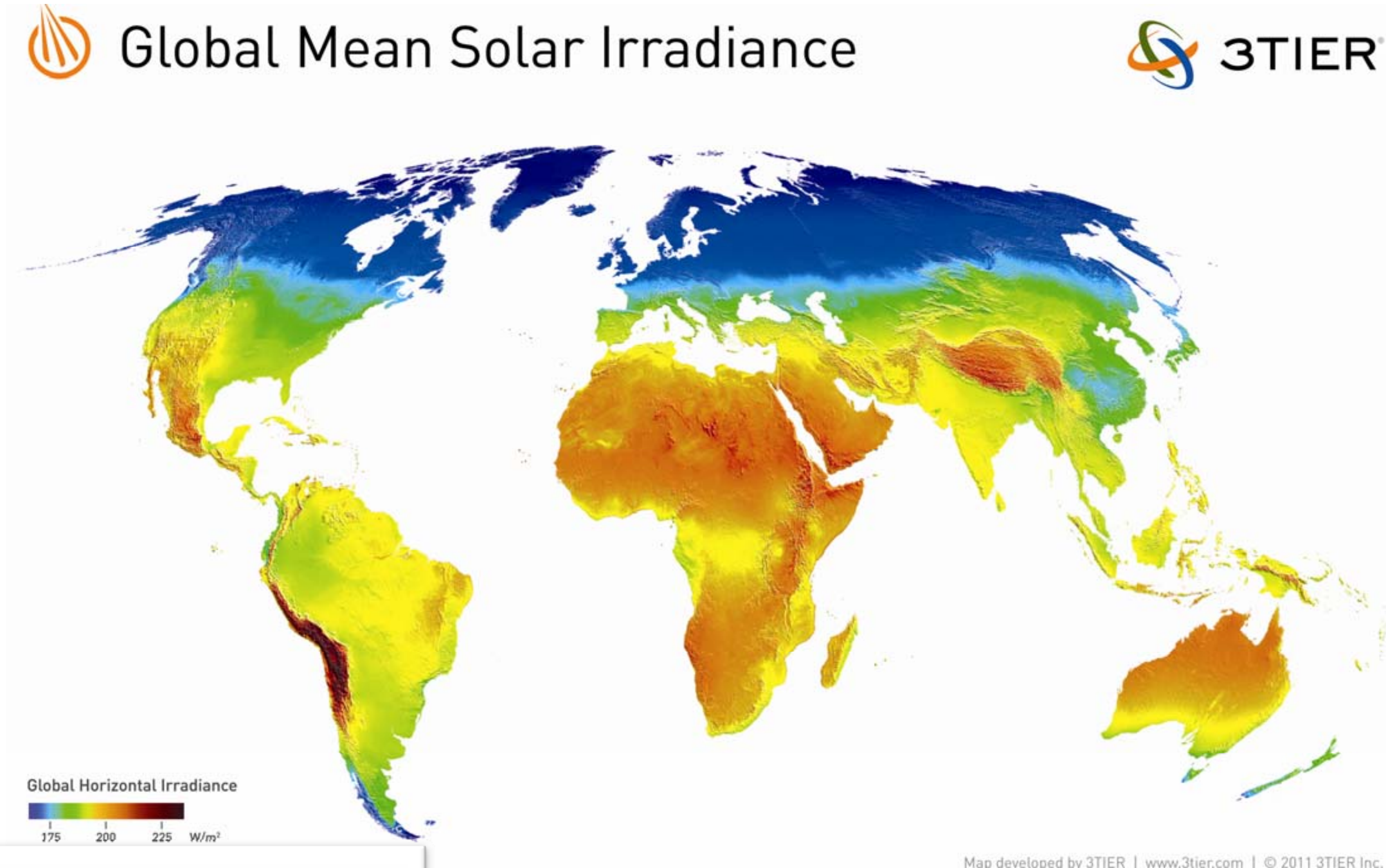
1W	50mW	1mW	100μW	50μW	1μW
5hours	24 hours	10 days		5 years	5 years

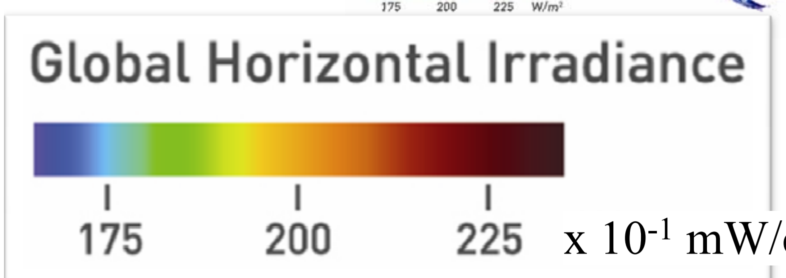
Ambient energy

R. J. M. Vullers, Zero-Power ICT Workshop 2009
R. J. M. Vullers *et al*, Solid-State Elec.**53**, 684 (2009)

Source	Source power	Harvested power
Ambient light		
Indoor	0.1 mW/cm^2	10 μW/cm^2
Outdoor	100 mW/cm^2	10 mW/cm^2
Vibration/motion		
Human	0.5 m @ 1 Hz 1 m/s^2 @ 50 Hz	4 μW/cm^2
Industrial	1 m @ 5 Hz 10 m/s^2 @ 1 kHz	100 μW/cm^2
Thermal energy		
Human	20 mW/cm^2	30 μW/cm^2
Industrial	100 mW/cm^2	1–10 mW/cm^2
RF		
Cell phone	0.3 μW/cm^2	0.1 μW/cm^2

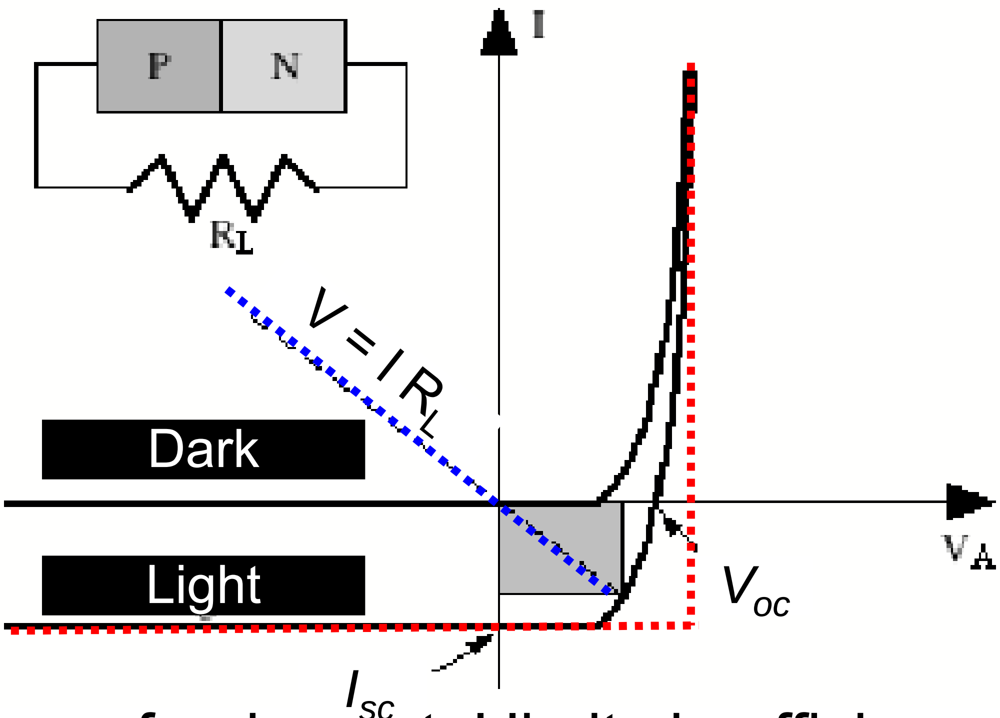
Radiance map





x 10^{-1} mW/cm^2

Operation point: intersection of the cell I-V characteristics with load line $V = I\,R_L$
Supplied power: shaded area



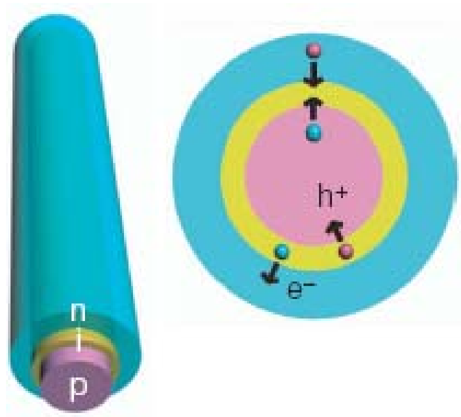
efficiency

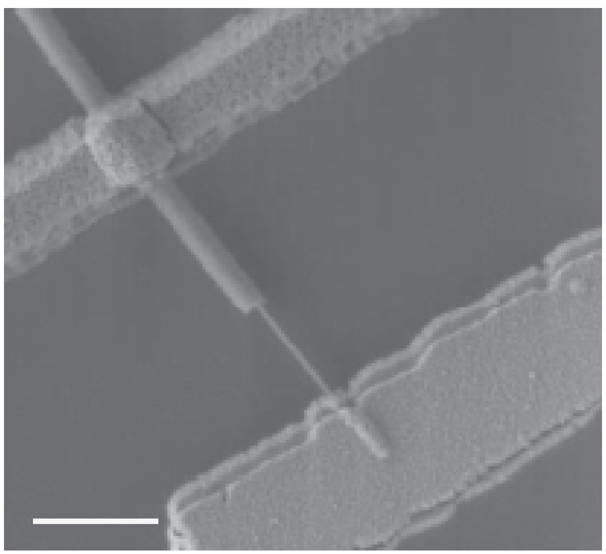
$$\eta = \frac{I_{sc} V_{oc} FF}{P_{in}}$$

I_{sc}: short circuit current
V_{oc}: open circuit voltage
FF: fill factor
P_{in}: incident power

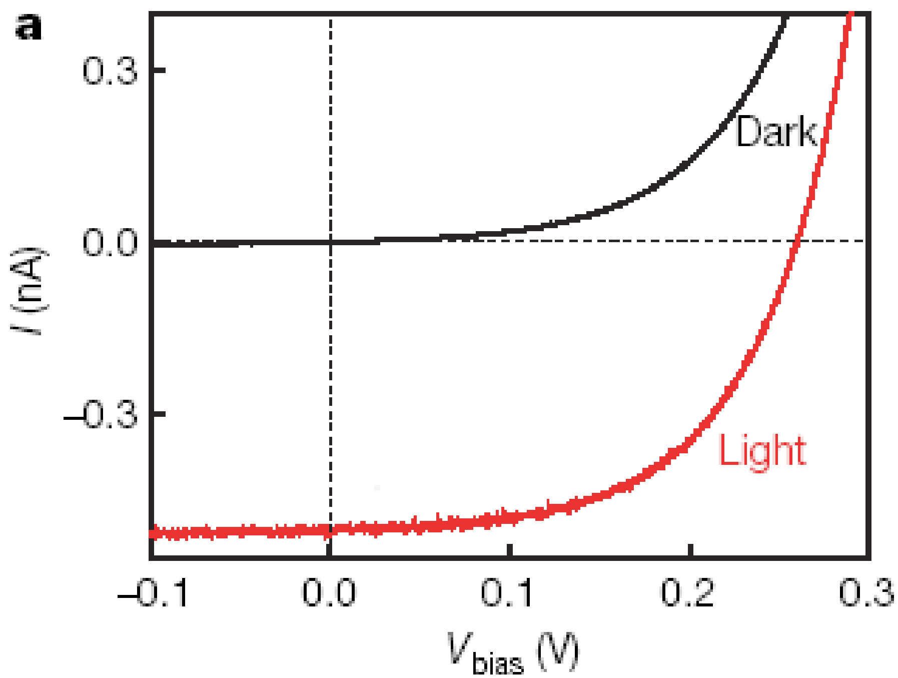
- fundamental limits in efficiency/obtained power
- I_{SC} depends on incident spectrum and "quantum efficiency"

Single nanowire coaxial cables





single p-i-n coaxial silicon nanowire
2.3%-3.4% efficiency delivering
200pW under 1-sun illumination

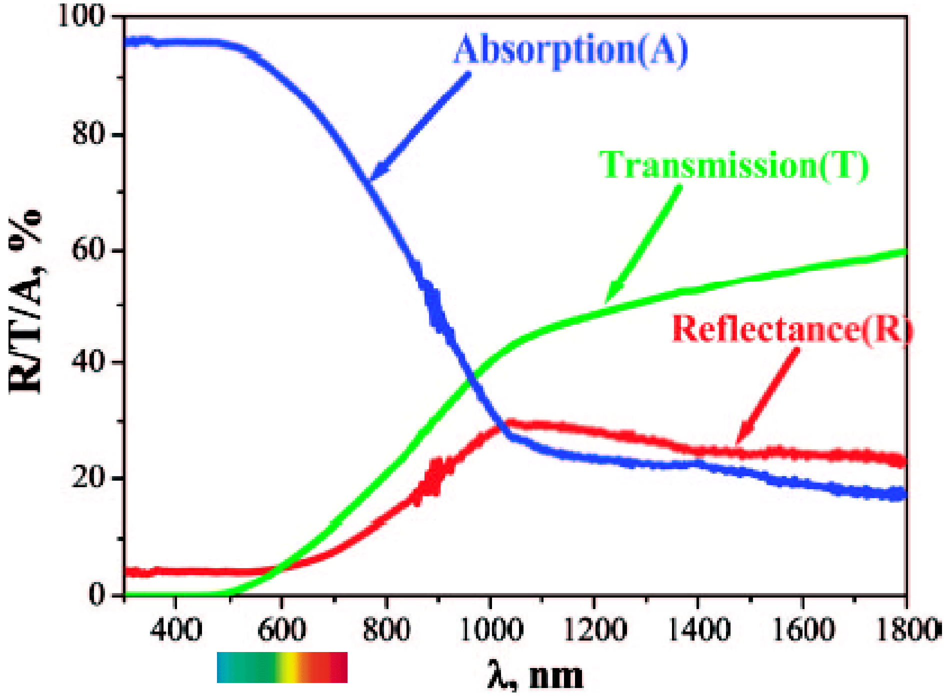


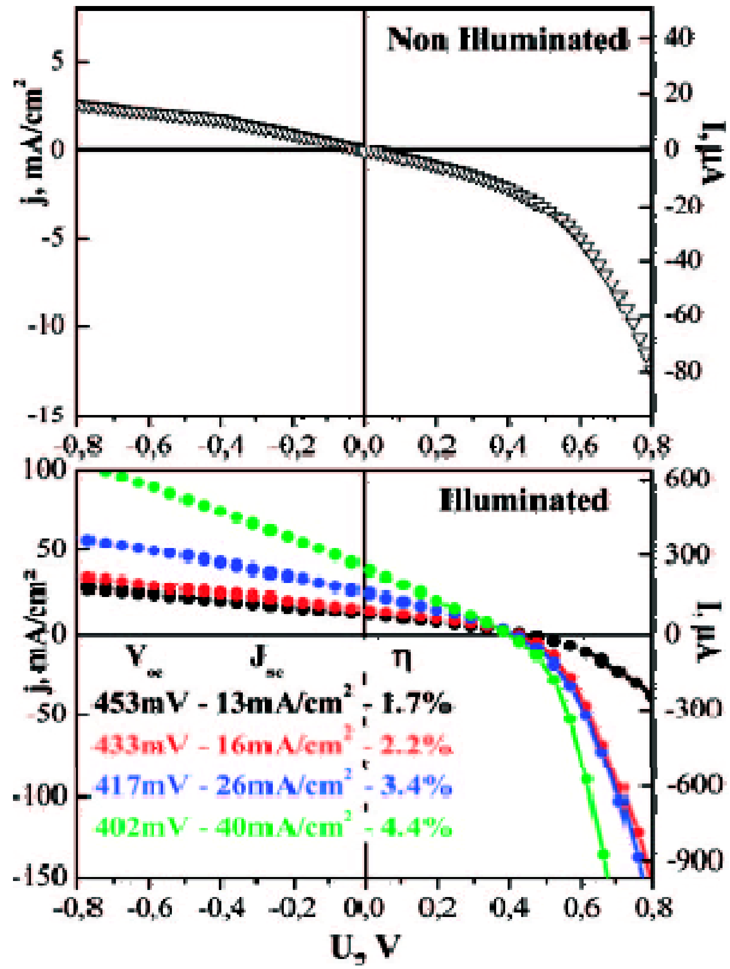
B. Tian, X. Zheng, T. J. Kempa1, Y. Fang, N. Yu, G. Yu, J. Huang & C. M. Lieber, Nature **449**, 885 (2007)

Axial junctions in nanowire arrays

antireflection effect in NW arrays

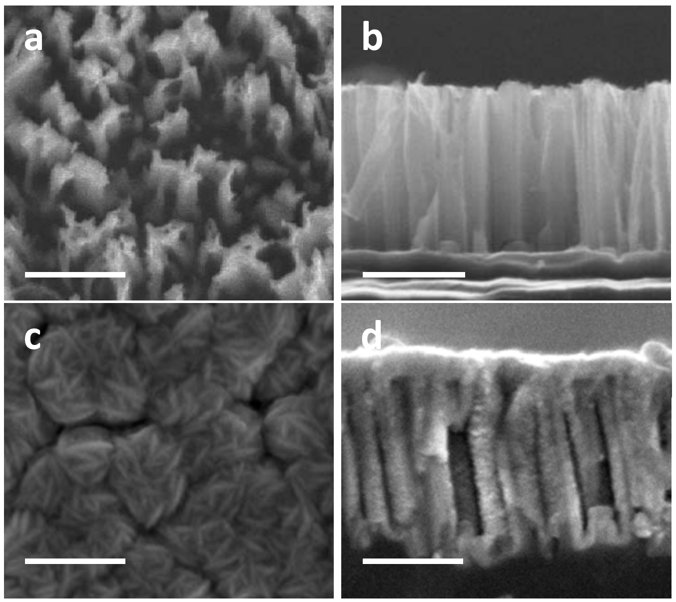
up to 4.4% efficiency under 1-sun illumination

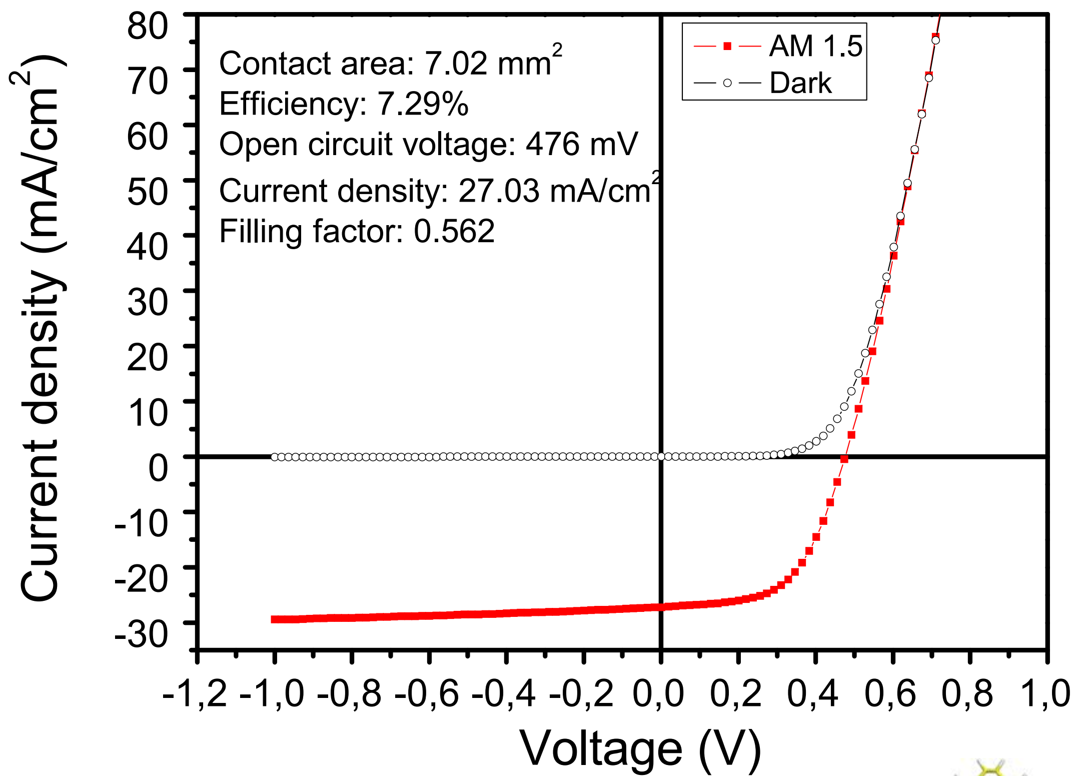




V. Sivakov, G. Andrä, A. Gawlik, A. Berger, J. Plentz, F. Falk, S.H. Christiansen, Nano Lett. **9**, 1549 (2009)

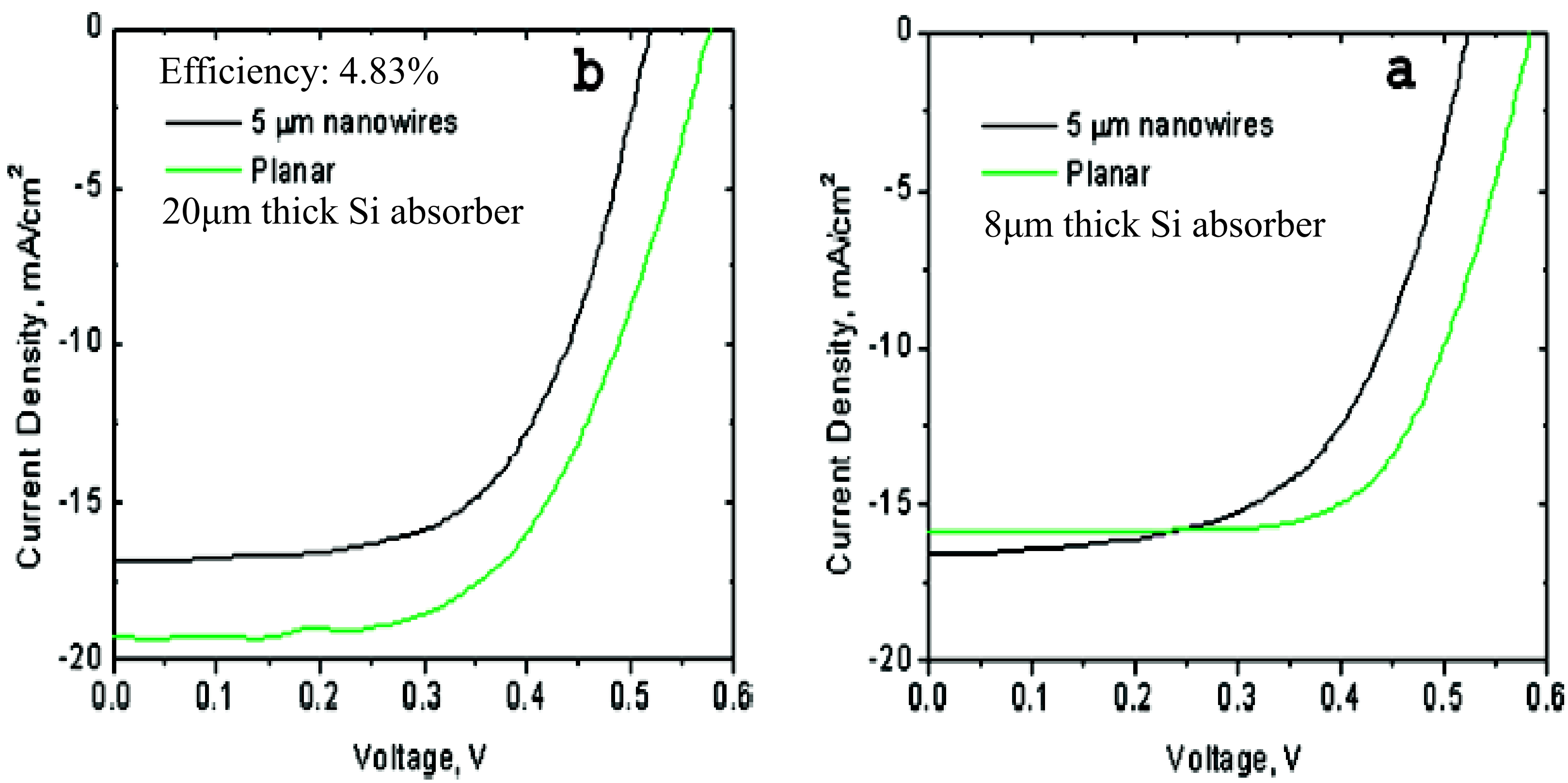
Arrays of nanowire coaxial cables





Guobin Jia, Martin Steglich, Ingo Sill, and Fritz Falk (IPHT), 2011

robust performance against thin film solar cells



Erik Garnett and Peidong Yang, Nano Lett. **10**, 1082 (2010)

How does it work?

Measure the conductivity response of nanowires as ions change electrostatics or as target molecules are adsorbed on the surface of nanowires

- avoids extra complexity of optical sensing
- lower cost
- easier to miniaturise

Why does the conductivity change?

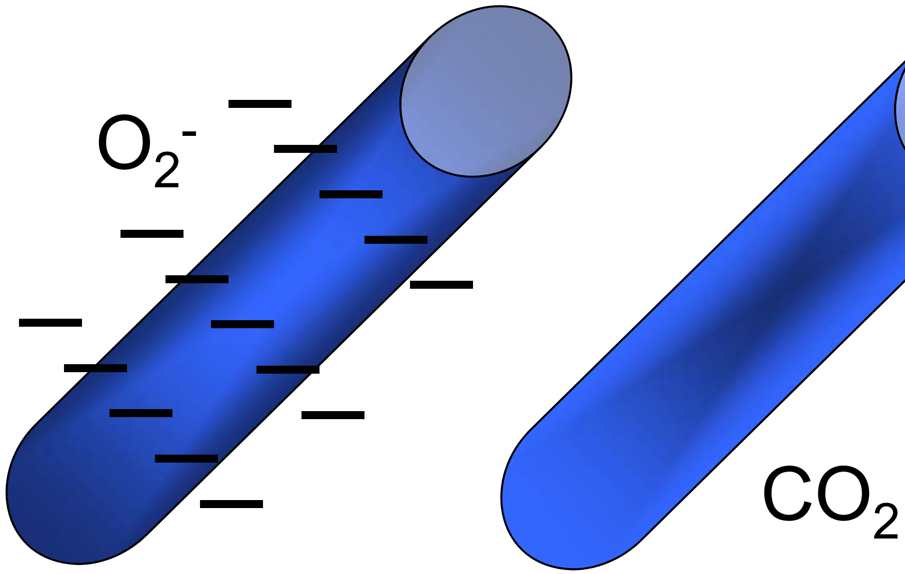
- chemically modulated field effect

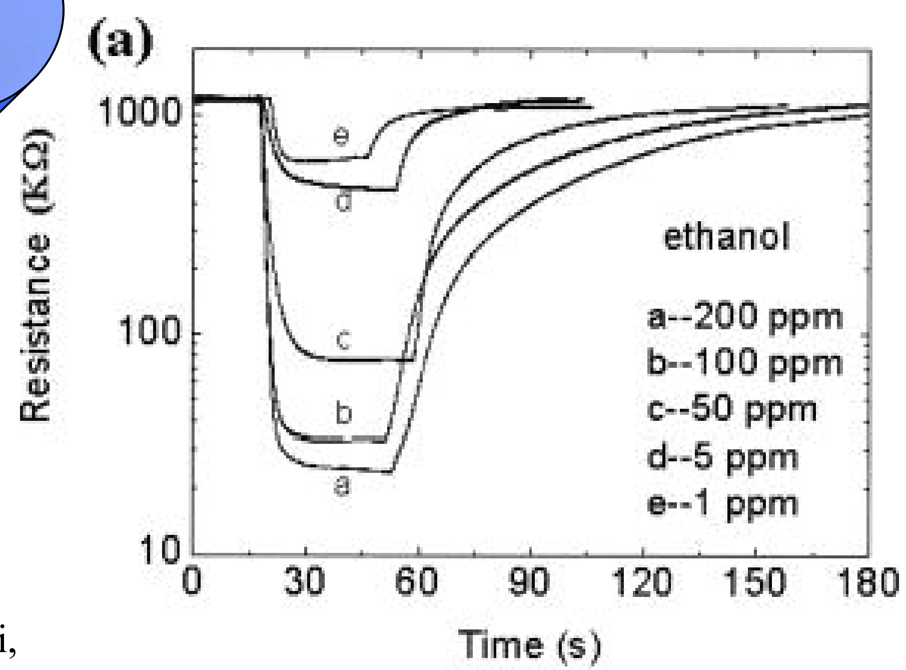
- charge carrier scattering and/or form change from adatoms

ethanol sensing with ZnO NWs down to 1ppm

ambient air
depletion of n-doped NW

ethanol enriched ambient
conducting channel

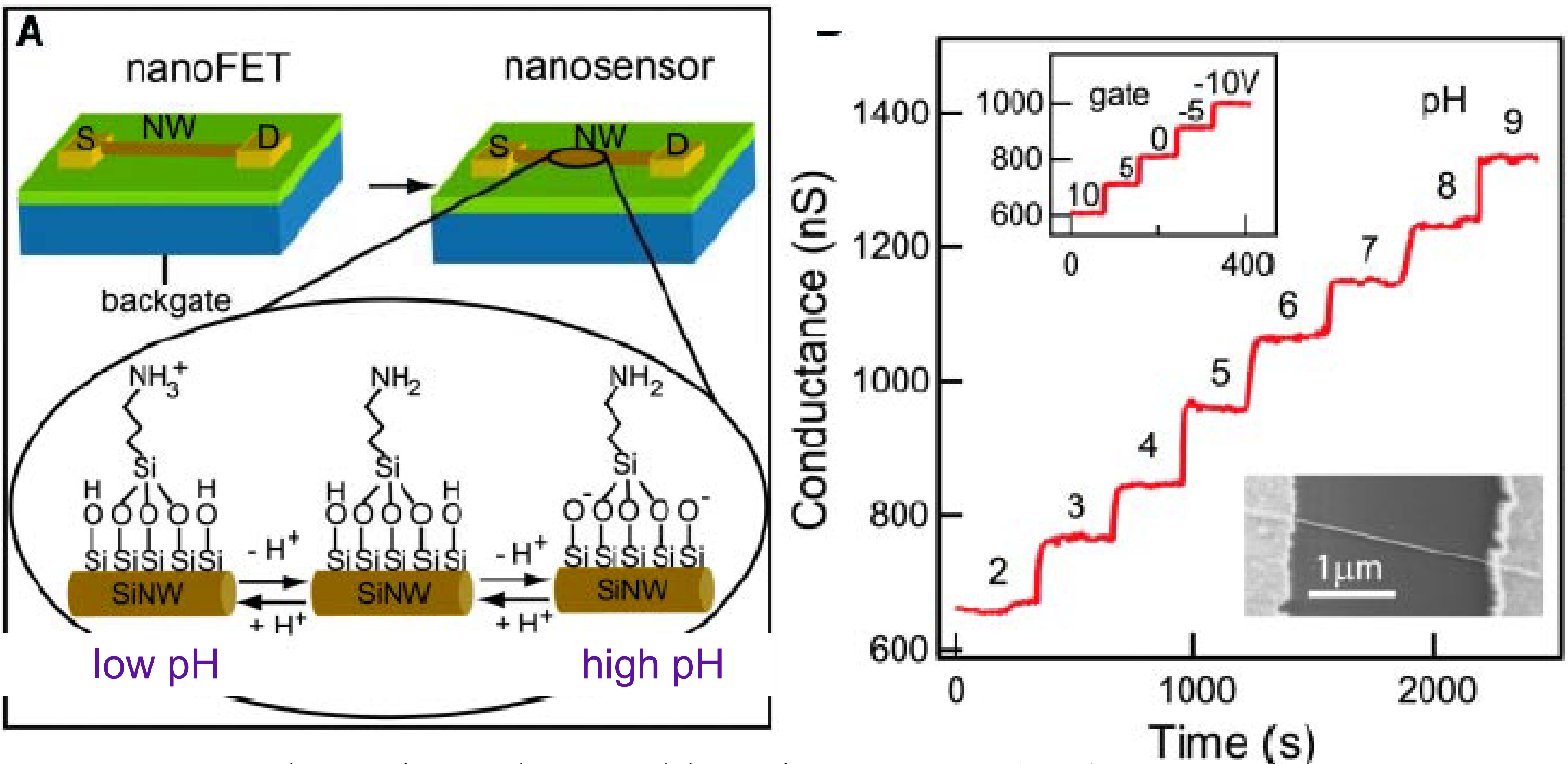




Q. Wan, Q. H. Li, Y. J. Chen, T. H. Wang, X. L. He, J. P. Li, and C. L. Lin, Appl. Phys. Lett. **84**, 3654 (2004)

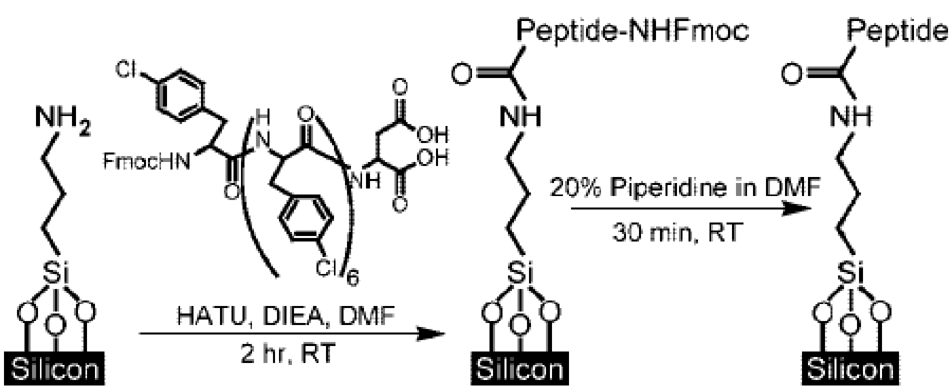
Nanowire-based sensors in solution

modified SiO_x surface with 3 aminopropyltriethoxysilane (APTES) to provide a surface that can undergo protonation and deprotonation, where changes in the surface charge can chemically gate the p-doped SiNW



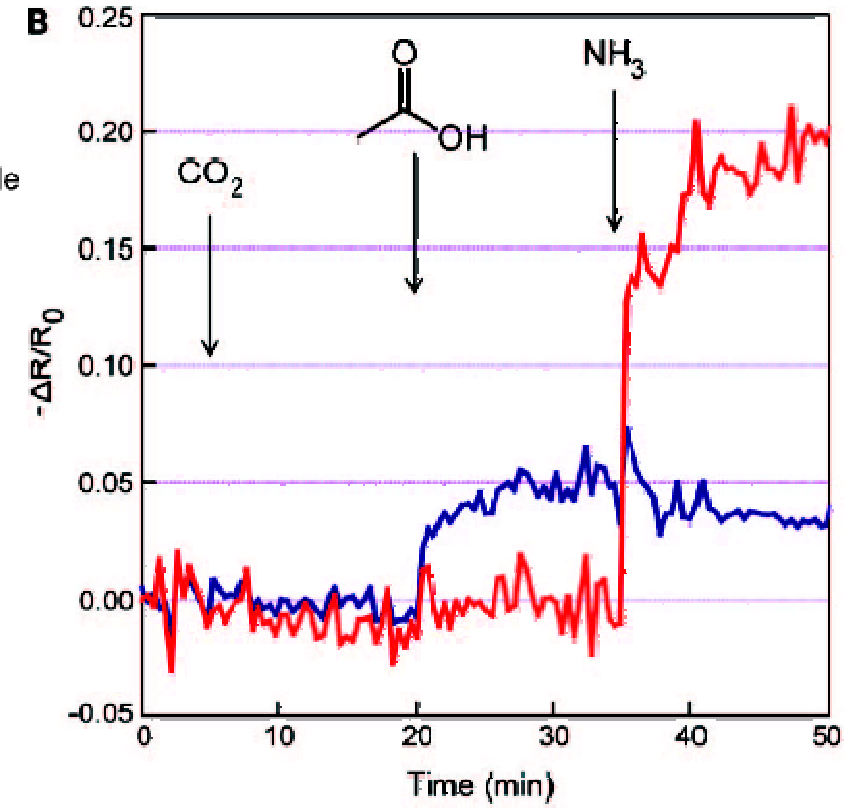
Y. Cui, Q. Wei, H. Park, C. M. Lieber, Science **293**, 1289 (2001)

Selectivity by covalent functionalisation



AcOH
asthma biomarker

kidney disease
biomarker

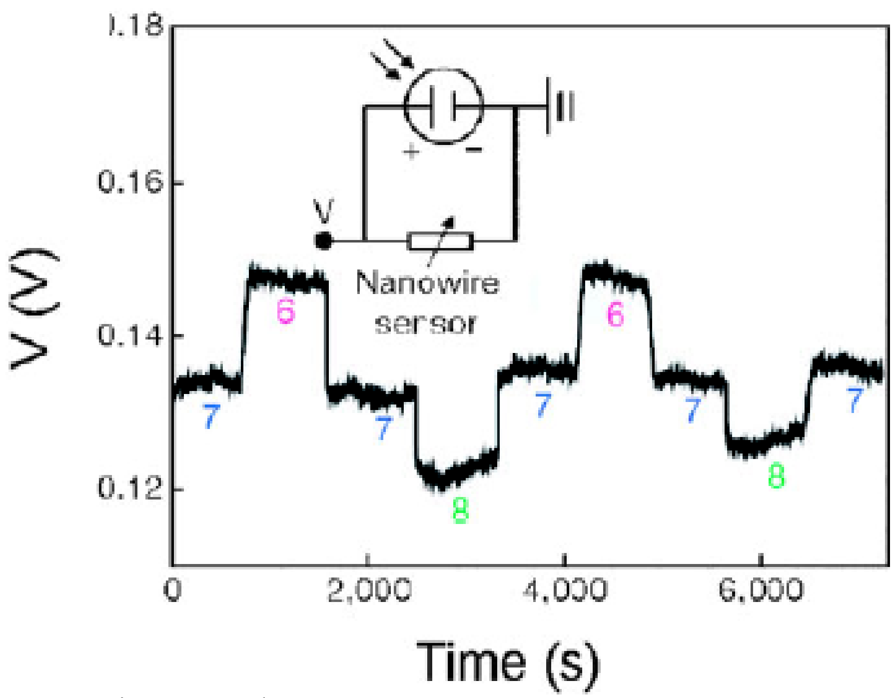


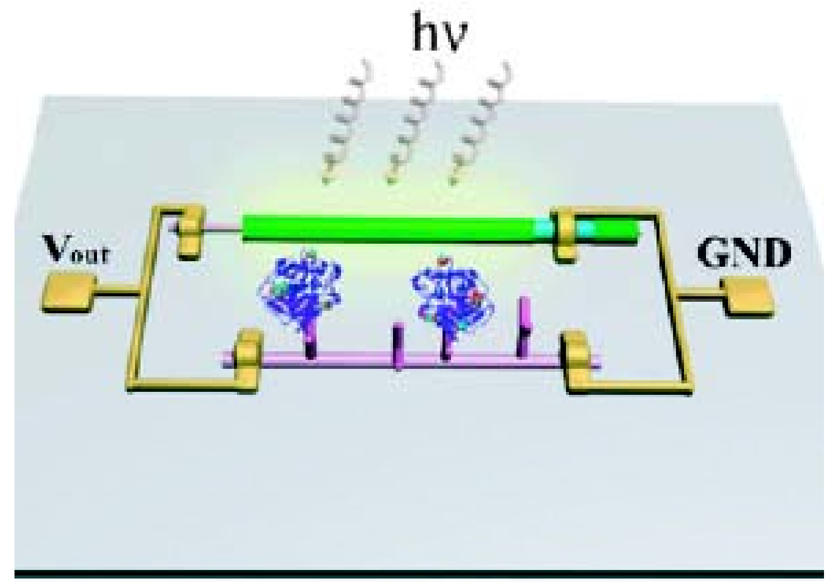
M.C. McAlpine *et al*, JACS **130**, 9583 (2008)

Autonomous sensing device

Proof-of-concept

powering of sensor units with single-NW PVs (10-100nW)

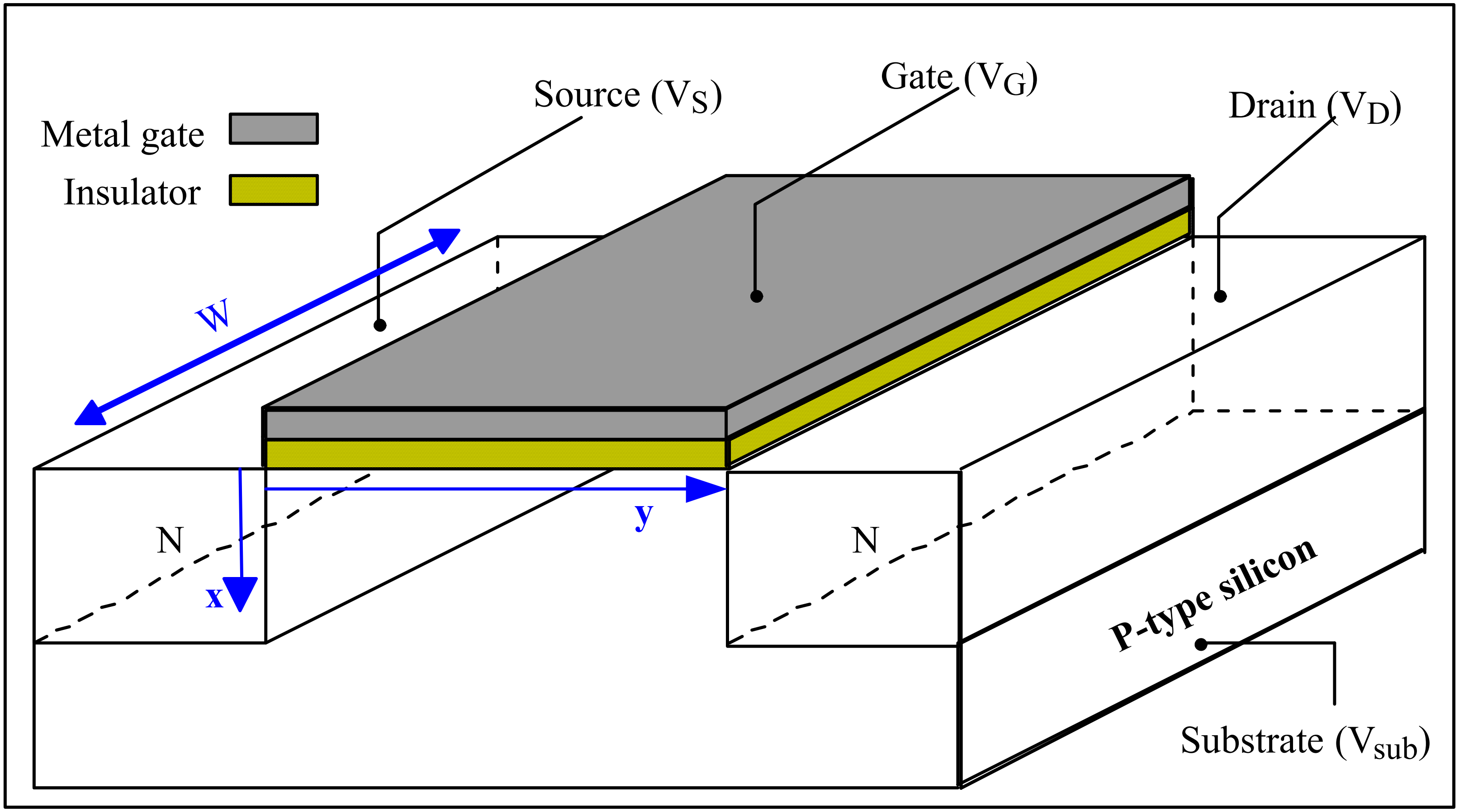




http://cmliris.harvard.edu/ Charles Lieber group

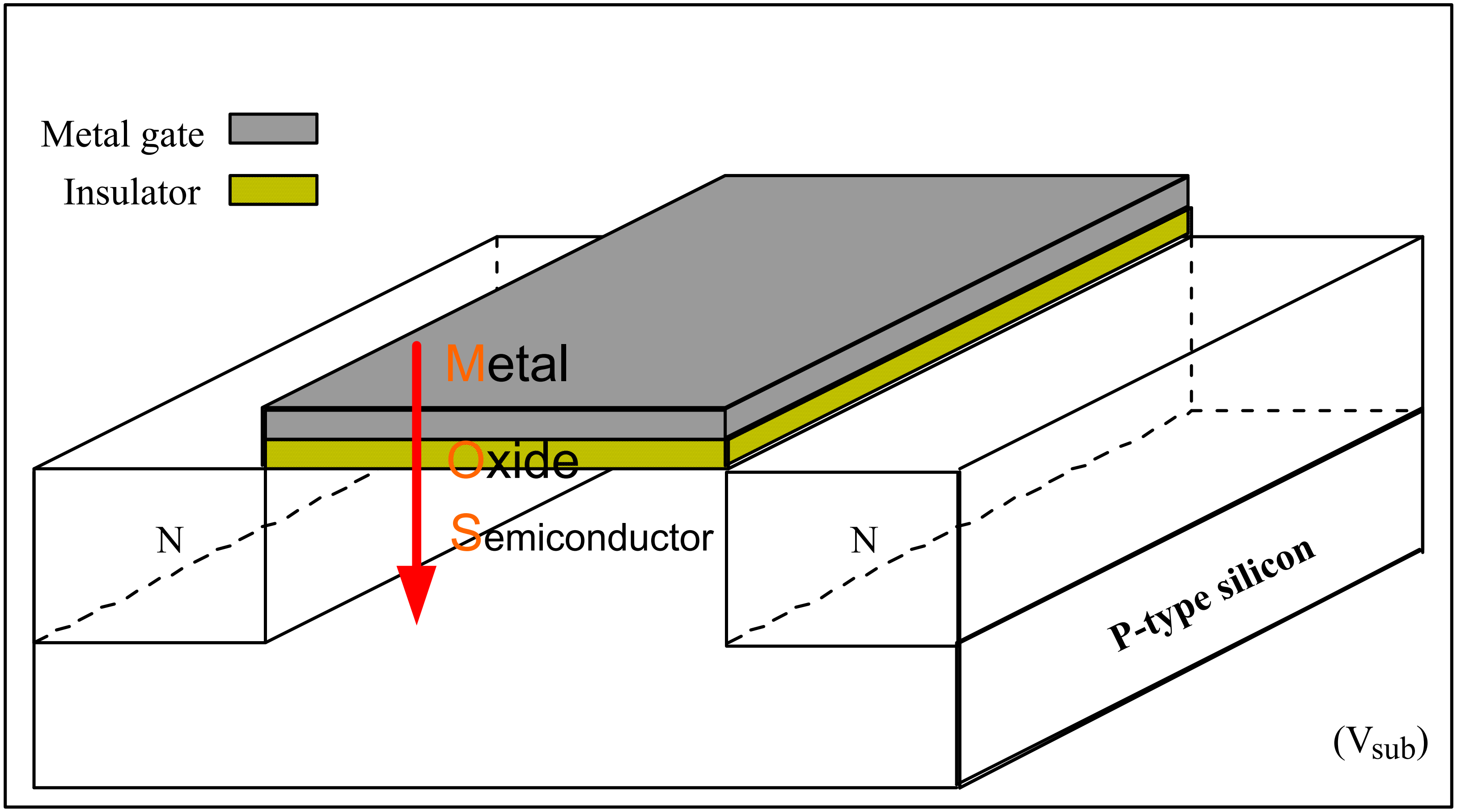
B. Tian, X. Zheng, T. J. Kempa1, Y. Fang, N. Yu, G. Yu, J. Huang & C. M. Lieber, Nature **449**, 885 (2007)
See also: S. Xu, Y. Qin, C. Xu, Y. Wei, R. Yang and Z. L. Wang, Nature Nanotech. **5**, 366 (2010)v

The MOS transistor: first approach



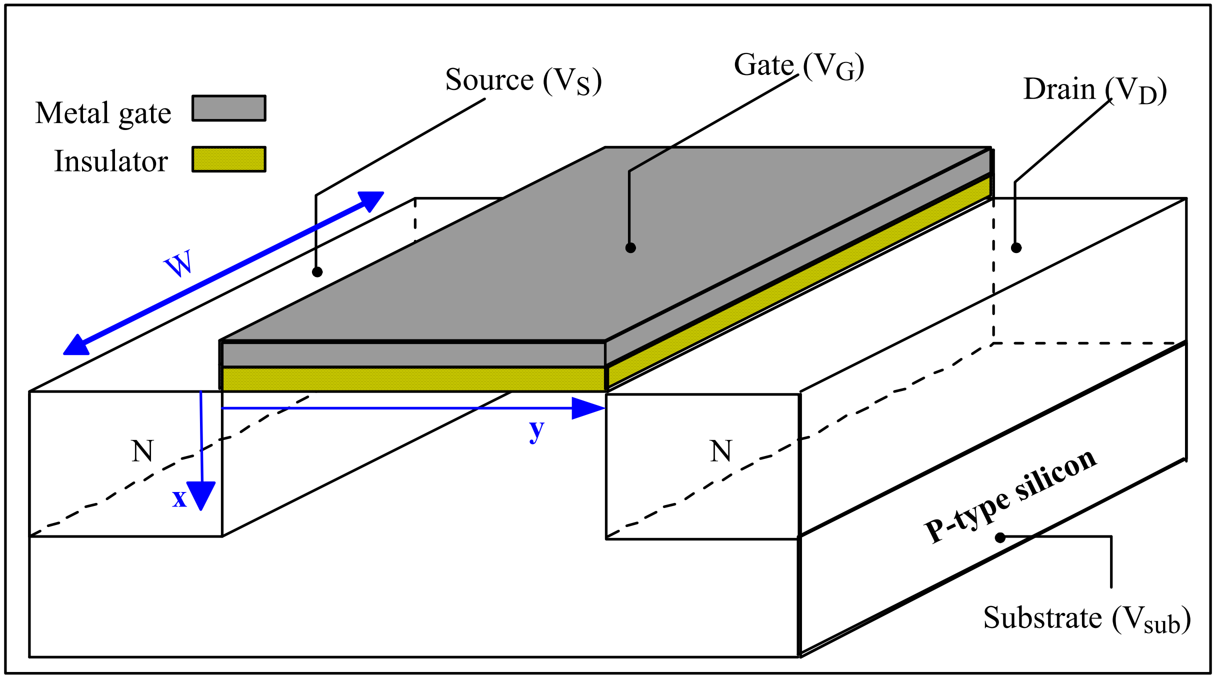
Courtesy J.-P. Colinge

The MOS transistor: first approach



Courtesy J.-P. Colinge

The MOS transistor: off state

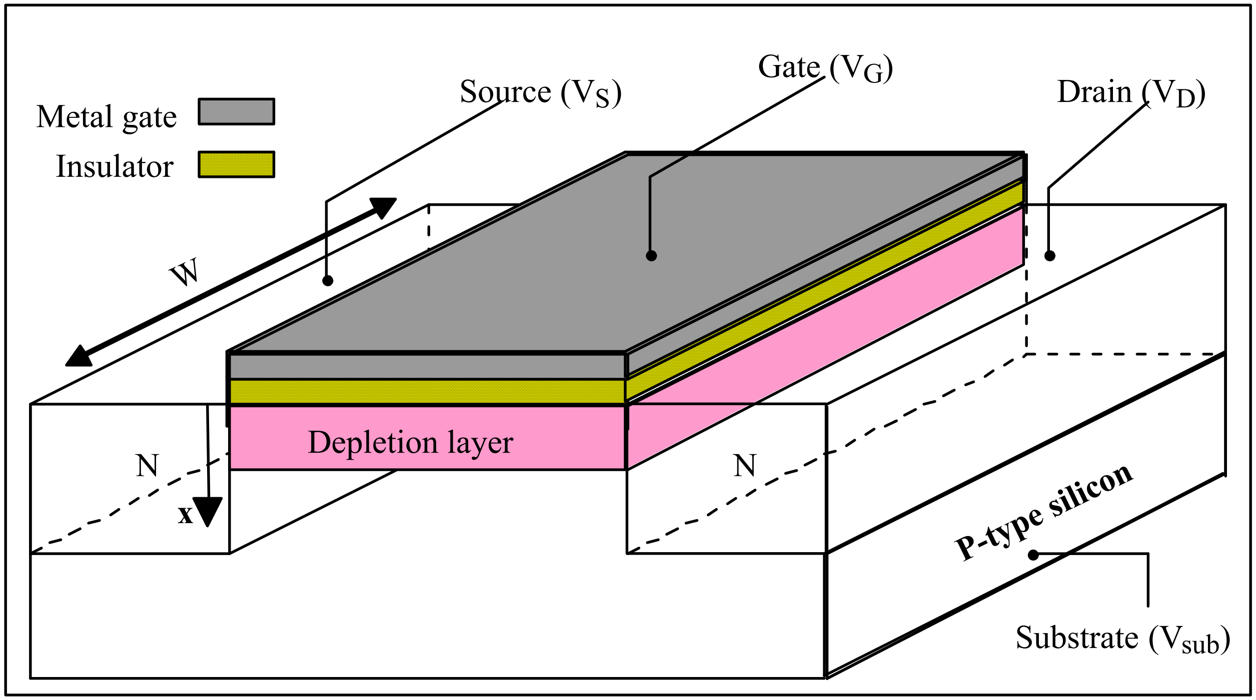


1: If the source and substrate are grounded there is no current in the source-substrate junction
2: If the drain voltage is positive the drain-substrate junction is reverse biased and there is no current in that junction
3: The gate is insulated from the rest of the device

Courtesy J.-P. Colinge

→ There is no current flowing in any of the terminals

The MOS transistor: off state → on state

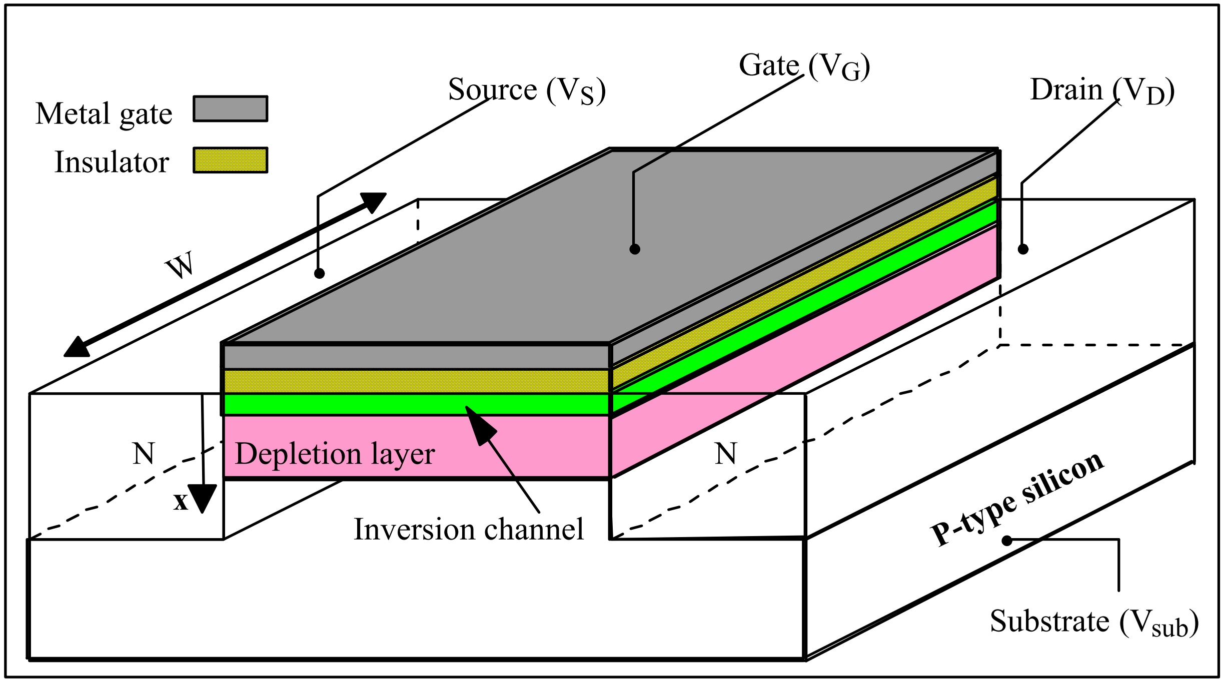


1: Positive gate voltage is applied. This repels free holes from the region under the oxide.
2: Junctions bias is unchanged, so there is no current in any of the terminals.

→ There is no current flowing in any of the terminals

Courtesy J.-P. Colinge

The MOS transistor: on state



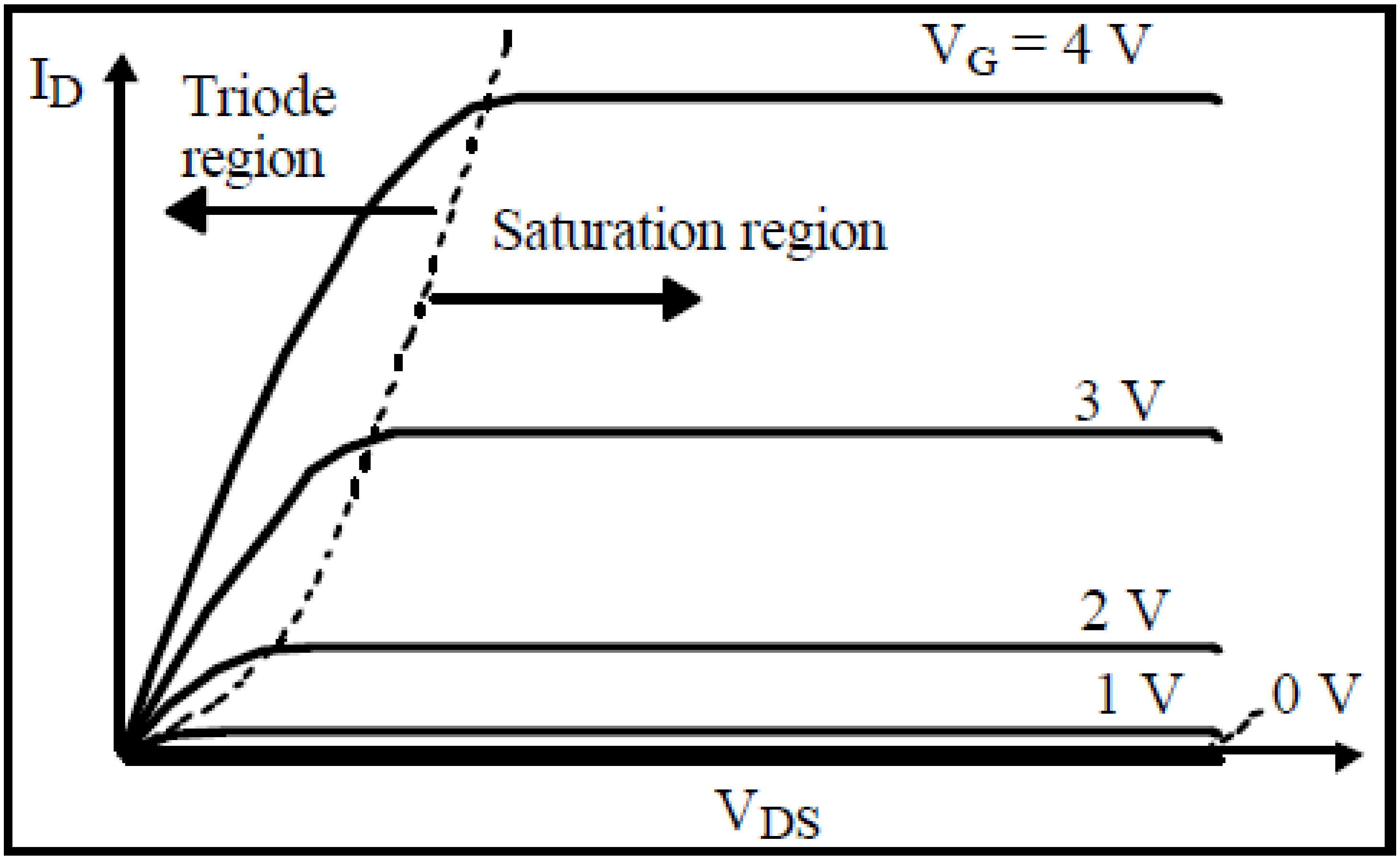
1: When a large enough positive gate voltage is applied electrons from the source are attracted underneath the gate oxide. (inversion layer)

2: An N-type layer called the "inversion channel" connects the N-type source to the N-type drain.

Courtesy J.-P. Colinge

→ Current flows from source to drain like in a resistor

Output characteristics



Courtesy J.-P. Colinge

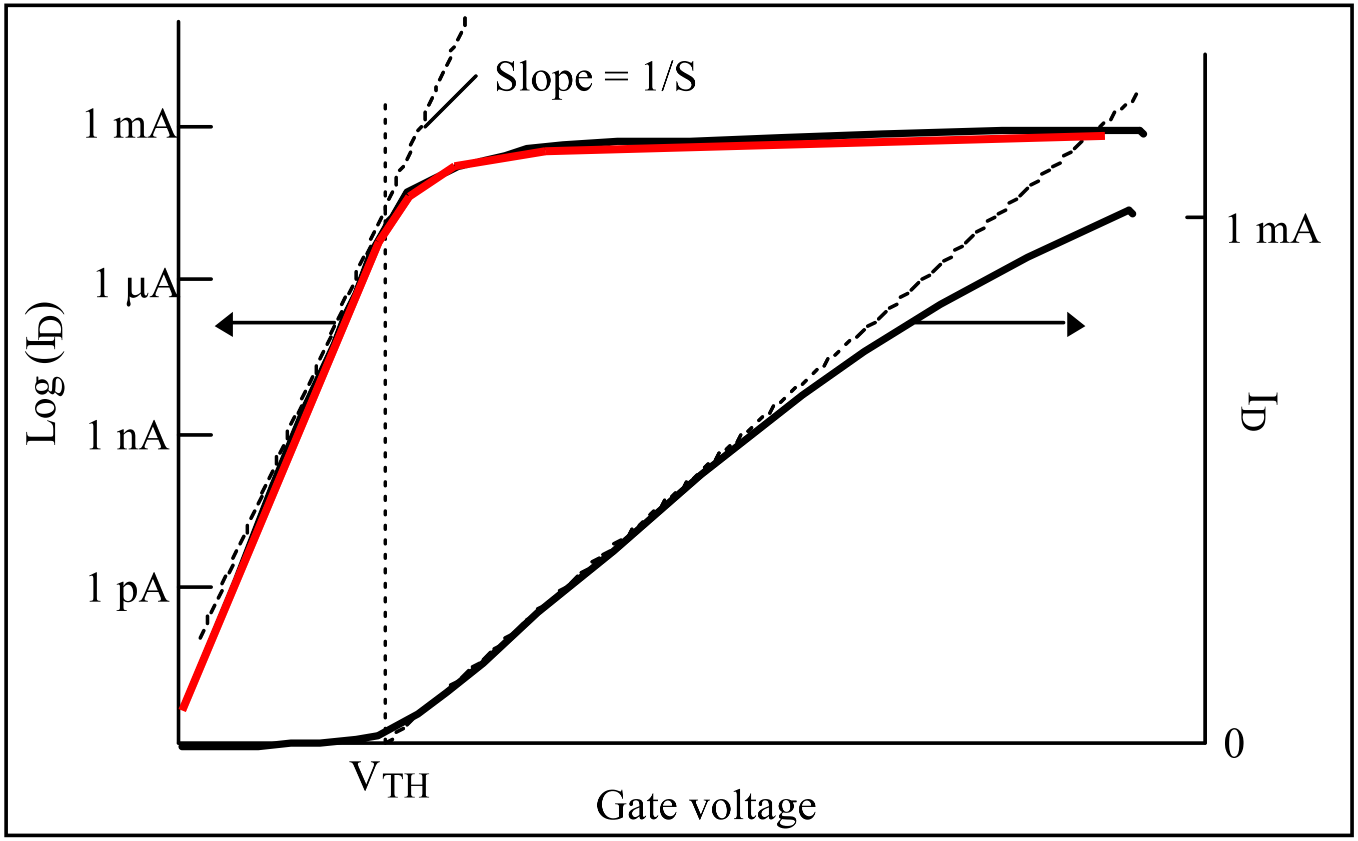
Basic MOSFET equations

- Triode $$I_D = \mu C_{ox} \frac{W}{L}\left[(V_G - V_{TH})V_D - \frac{1}{2} n V_D^2\right]$$
- Saturation $$I_{Dsat} = \frac{1}{2n}\mu\, C_{ox}\frac{W}{L}(V_G - V_{TH})^2$$
- Subthreshold swing $$S = n\frac{kT}{q}\ln(10)$$
- Reduced transconductance $$\frac{g_m}{I_D} = \sqrt{\frac{2\mu C_{ox} W/L}{n I_D}}$$

Courtesy J.-P. Colinge

n is the BODY EFFECT COEFFICIENT, *aka.* BODY FACTOR
It is often neglected (n=1) in simplified models… but it is definitely present in real devices.

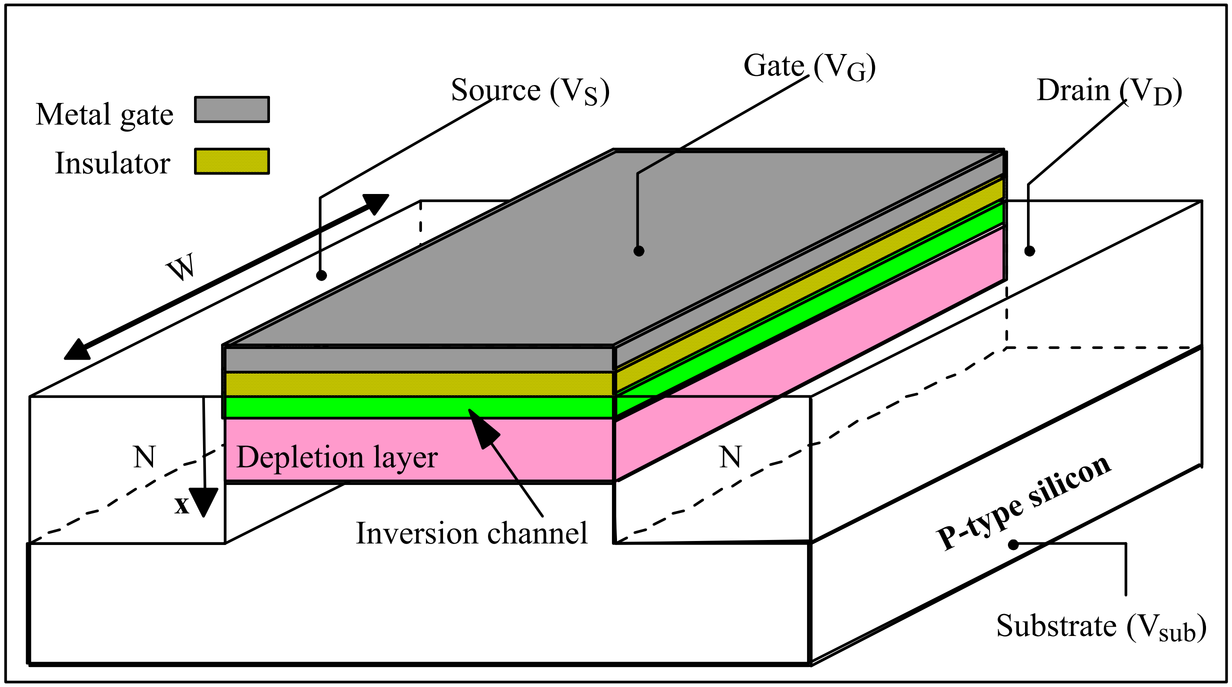
Current below threshold (subthreshold slope, S)

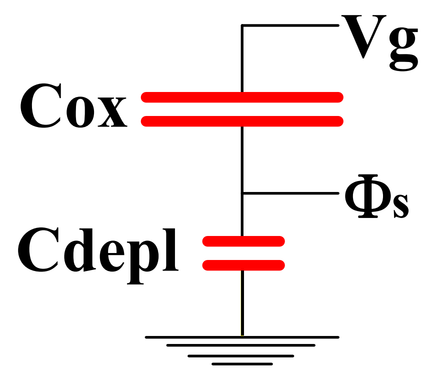


Courtesy J.-P. Colinge

The smaller the value of *S*, the better!
– the "faster" the devices switches from off to on

Gate-to-channel coupling; Body Effect





$$\left\{ \begin{array}{l} dQ_{bottom} = C_{depl}\, d\Phi_S \\ dQ_{top} = C_{ox}\, d\left(V_g - \Phi_S\right) \end{array} \right.$$

$$C_{ox}\left(dV_g - d\Phi_S\right) = C_{depl}\, d\Phi_S$$

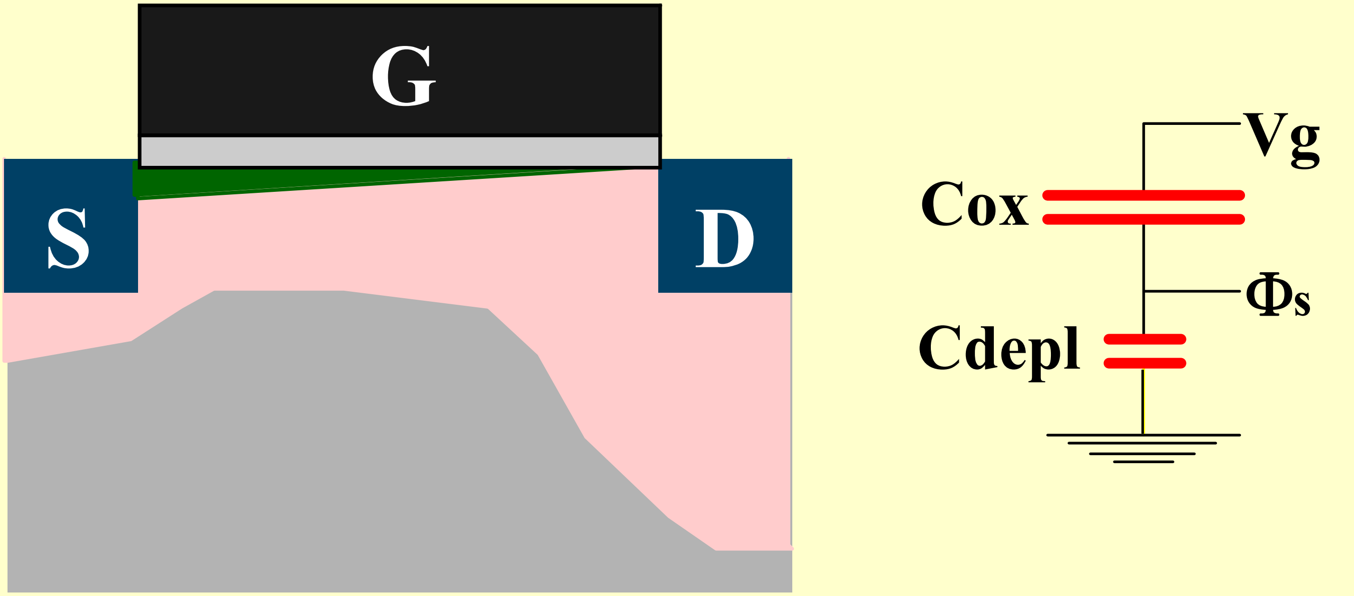
$$\frac{dV_g}{d\Phi_S} = \frac{C_{ox} + C_{depl}}{C_{ox}} = 1 + \frac{C_{depl}}{C_{ox}} \equiv n$$

Courtesy J.-P. Colinge

$n =$ Body Factor

Gate-to-channel coupling; Body Effect

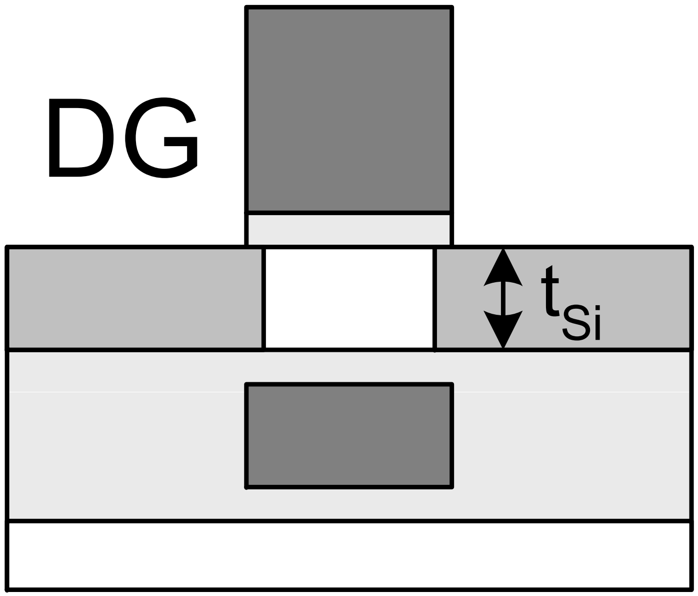
$$n \equiv \frac{dV_G}{d\Phi_S} = \frac{C_{ox} + C_{depl}}{C_{ox}} = 1 + \frac{C_{depl}}{C_{ox}} = 1 + \frac{C_{channel\ to\,ground}}{C_{channel\ to\,gate}}$$

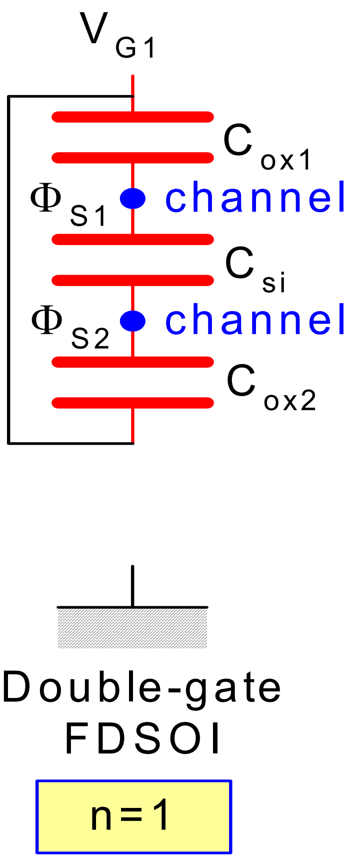


Body factor: n = …1.5… in a Bulk MOSFET

Courtesy J.-P. Colinge

The DGMOS transistor: n=1





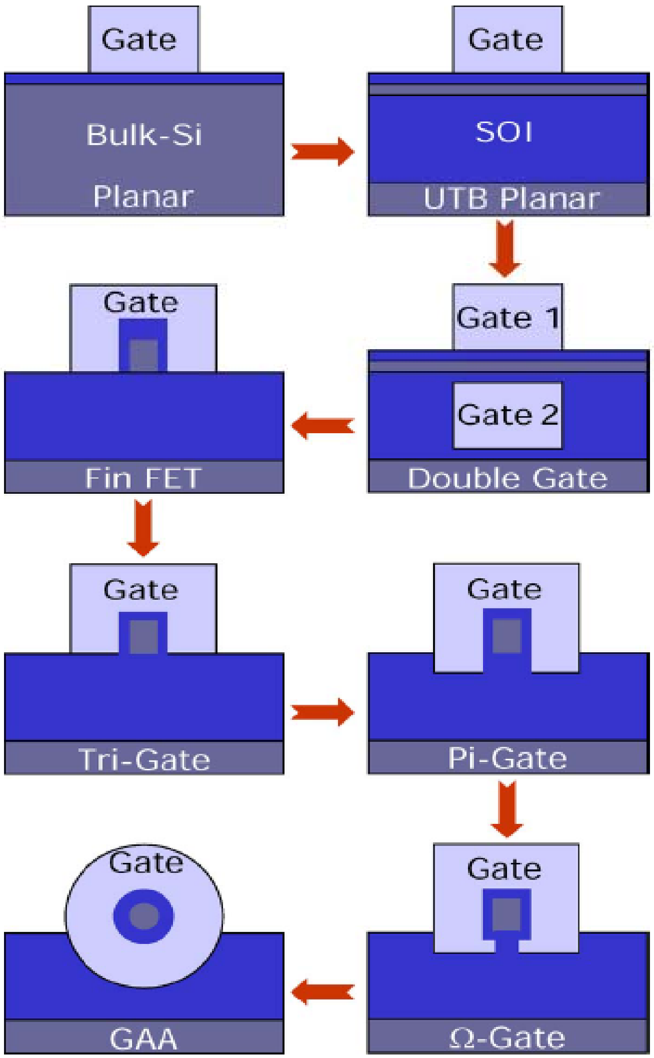
DGMOS transistor: Double-Gate MOS Transistor

$$\frac{dV_g}{d\Phi_s} = n = 1$$

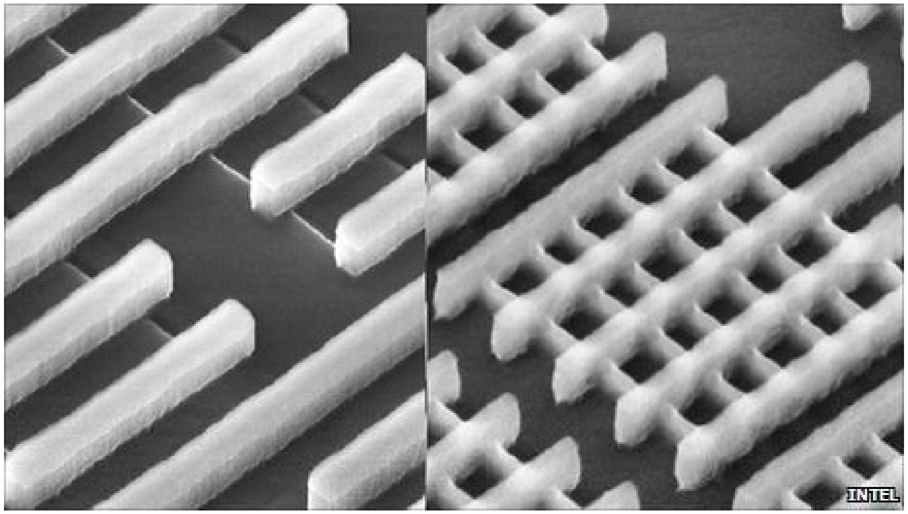
Courtesy J.-P. Colinge

Transistor scaling
why nanowires?

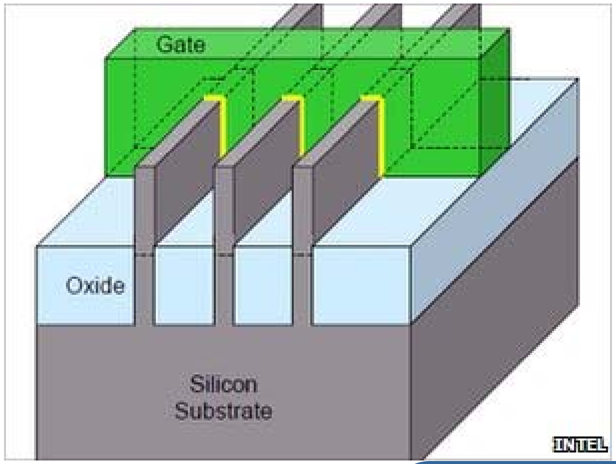
transistor progression

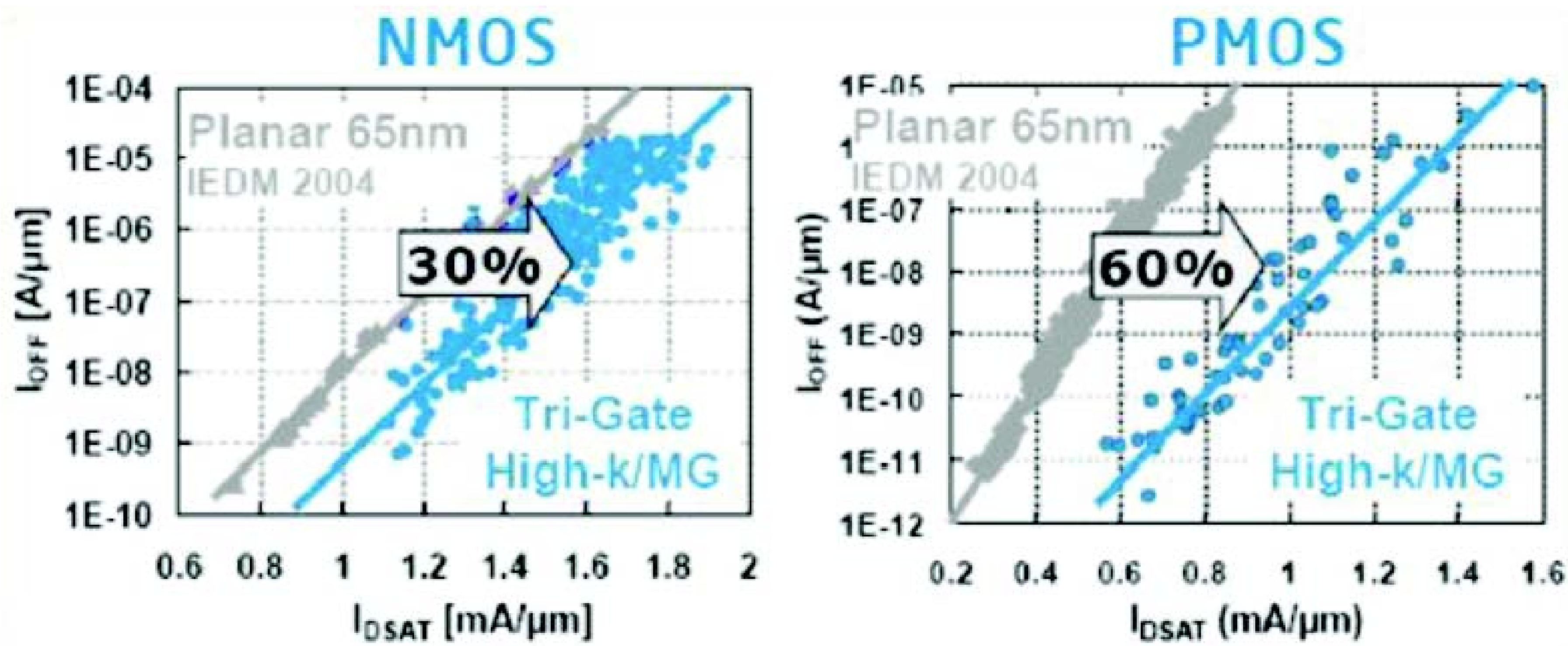


Sing *et al*, IEEE TED **55**, 3107 (2008)



Intel 22nm Ivy Bridge (2011)

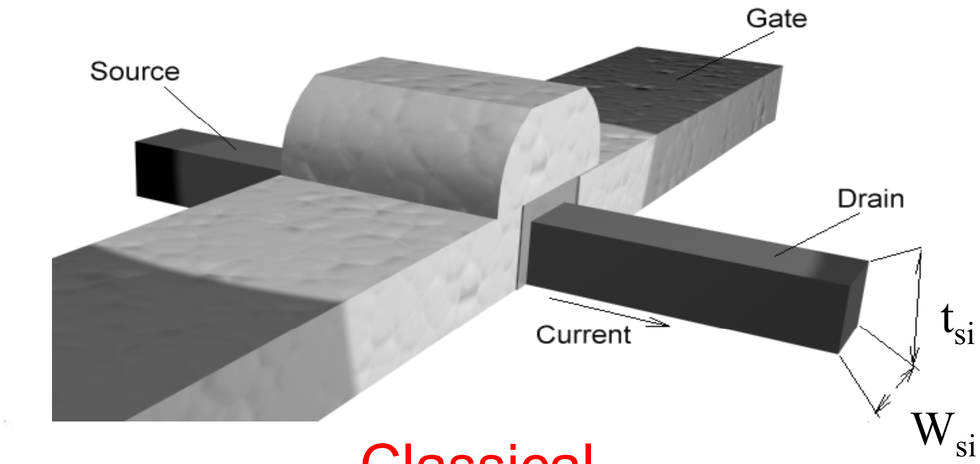


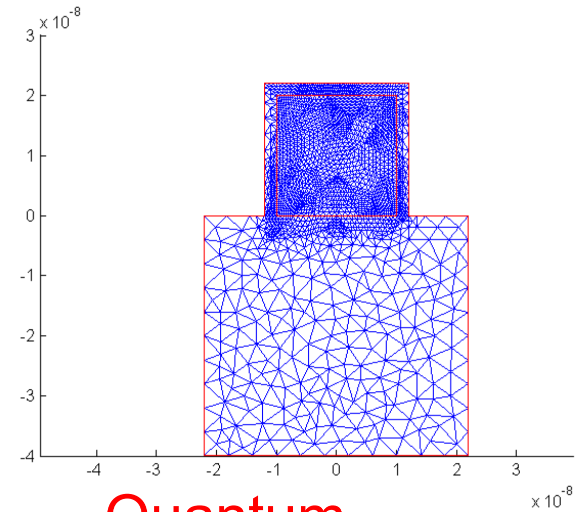


R. S. Chau,
Technology@Intel Magazine (2006)

Above threshold:
large cross section

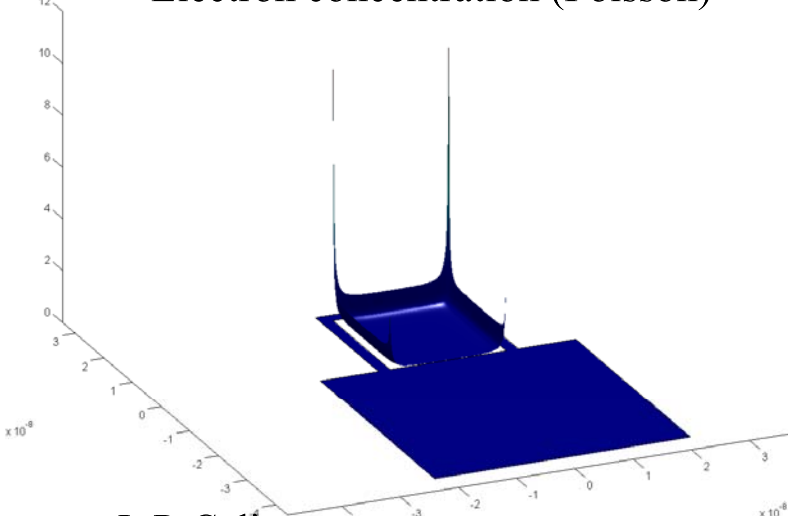
$W_{si}=t_{si}=$**20 nm**, $N_a=5x10^{17}\ cm^{-3}$





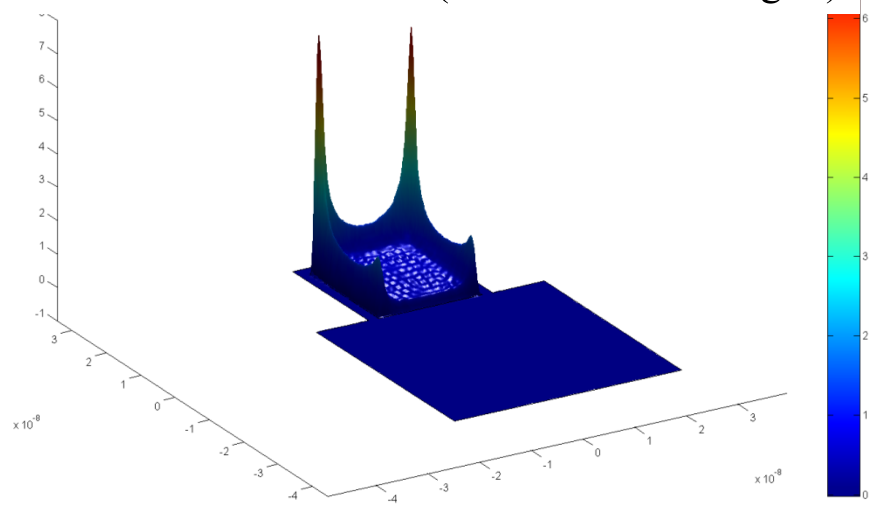
Classical

Electron concentration (Poisson)



Quantum

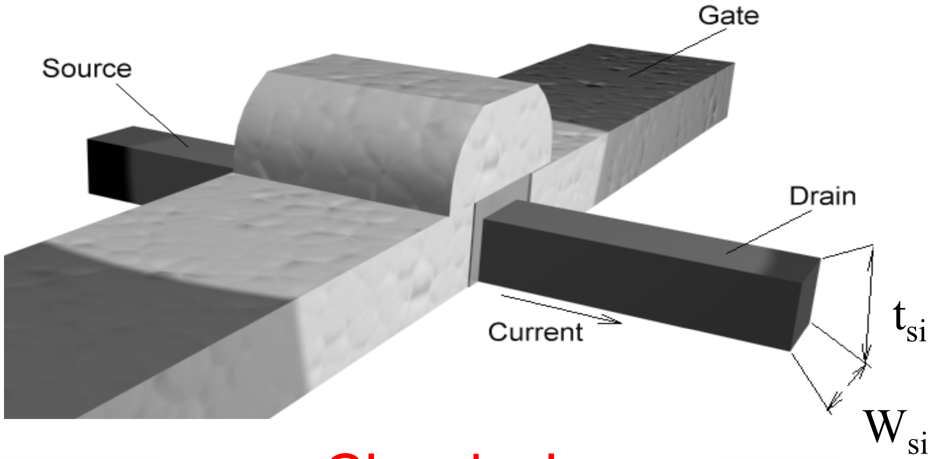
Electron concentration (Poisson+Schrödinger)

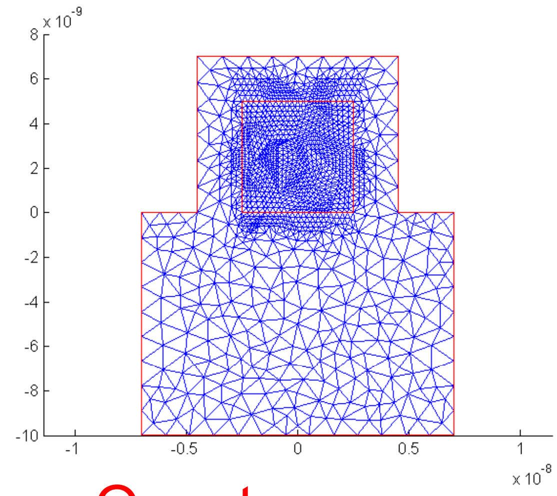


Courtesy J.-P. Colinge

Below threshold: small cross section

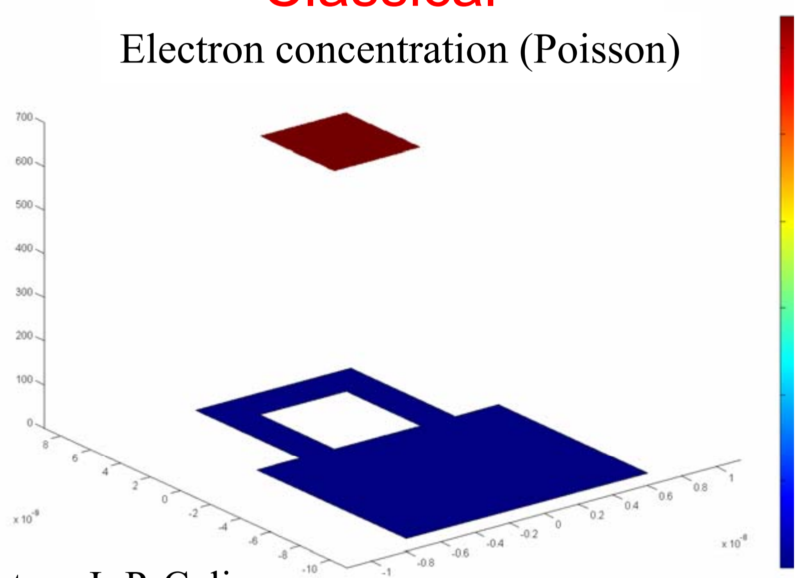
$W_{si}=t_{si}=$ **5 nm**, $N_a=5\times10^{17}\ cm^{-3}$





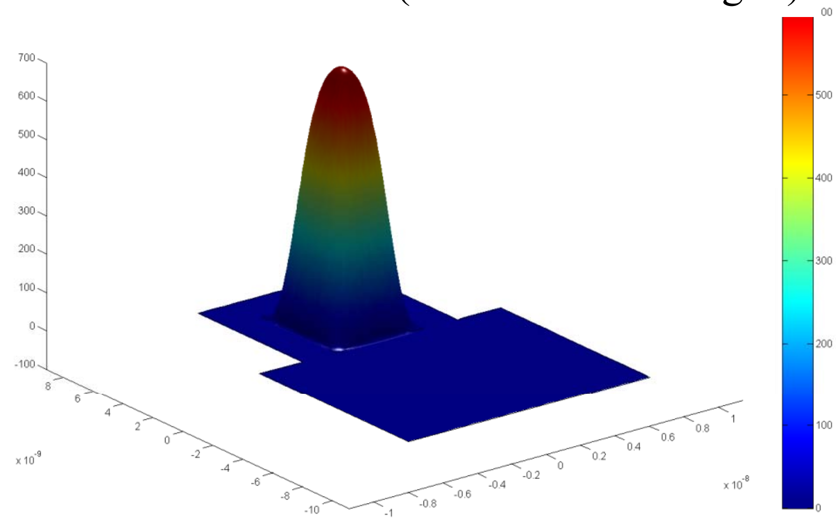
Classical

Electron concentration (Poisson)



Quantum

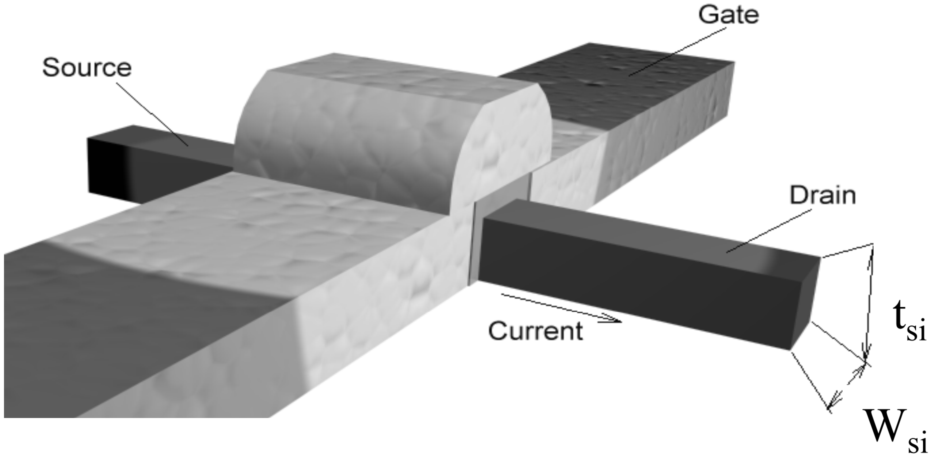
Electron concentration (Poisson+Schrödinger)

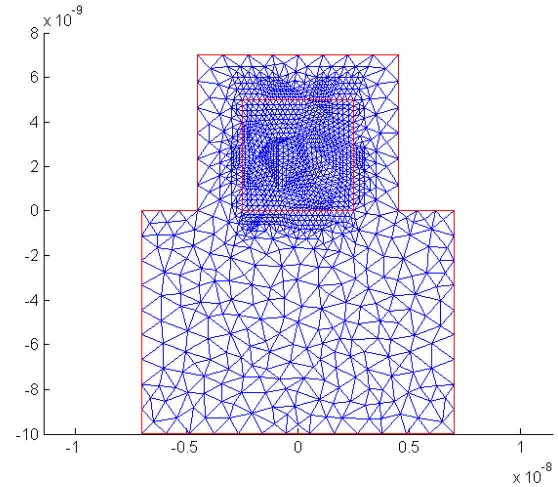


Courtesy J.-P. Colinge

Above threshold:
small cross section

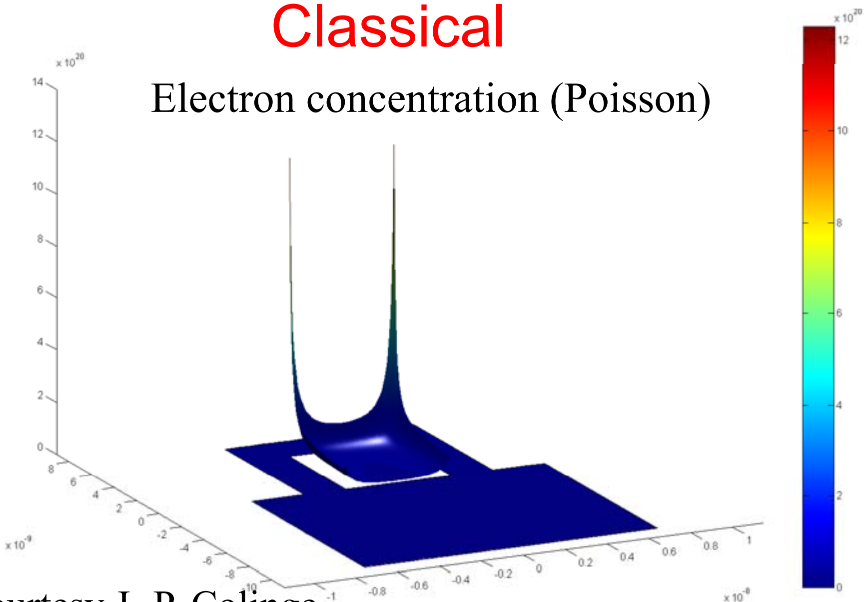
$W_{si}=t_{si}=$ **5 nm**, $N_a=5x10^{17}\ cm^{-3}$





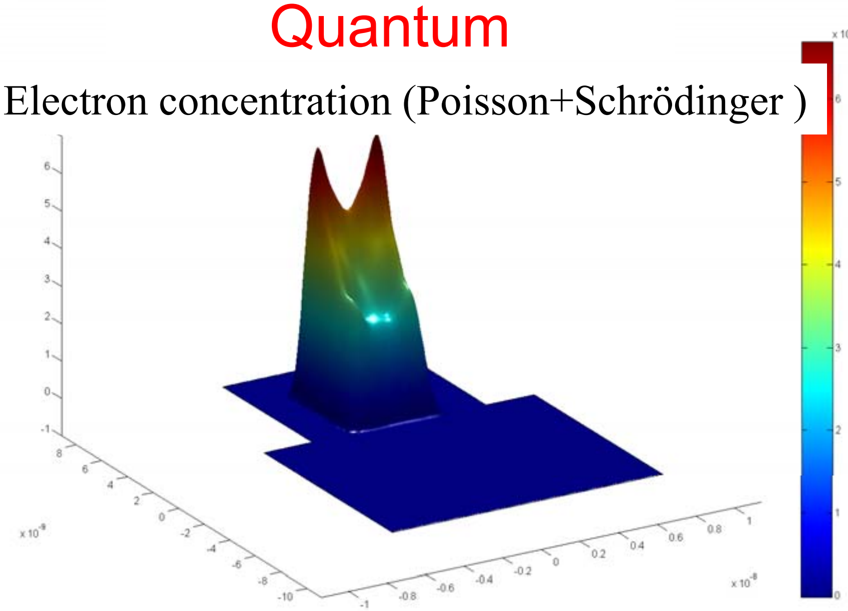
Classical

Electron concentration (Poisson)



Quantum

Electron concentration (Poisson+Schrödinger)



Courtesy J.-P. Colinge

Why nanowires?

Scientifically interesting

- large surface to volume ratio
- surface chemistry can influence electronic properties
- quantum effects
- multi-functionality

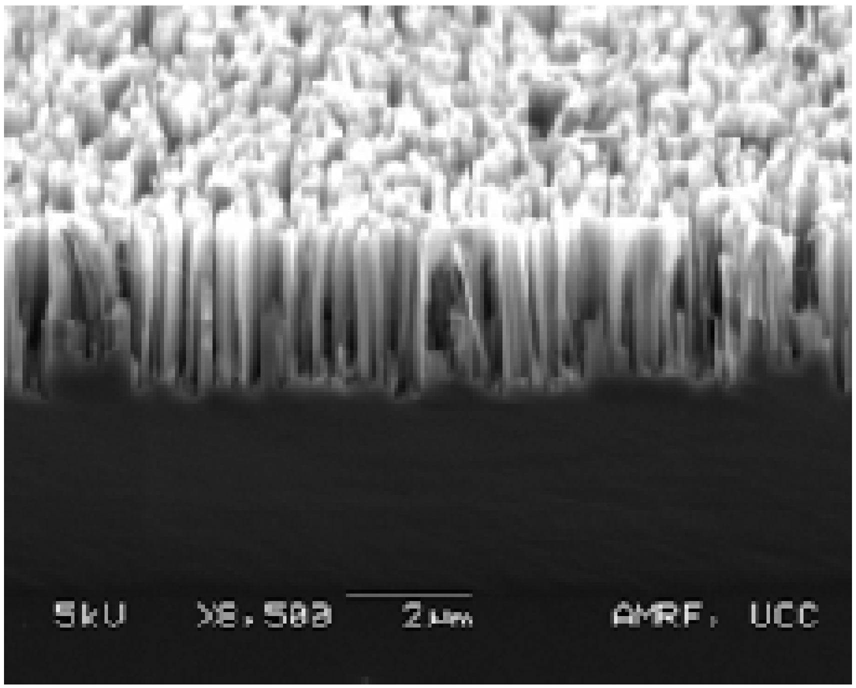
Technologically relevant

- energy harvesters (photovoltaics, thermoelectric, mechanical)
- (bio-)chemical nanosensors
- field-effect transistors
- light-emitting diodes and lasers…

Fabrication methods

“Top-down”

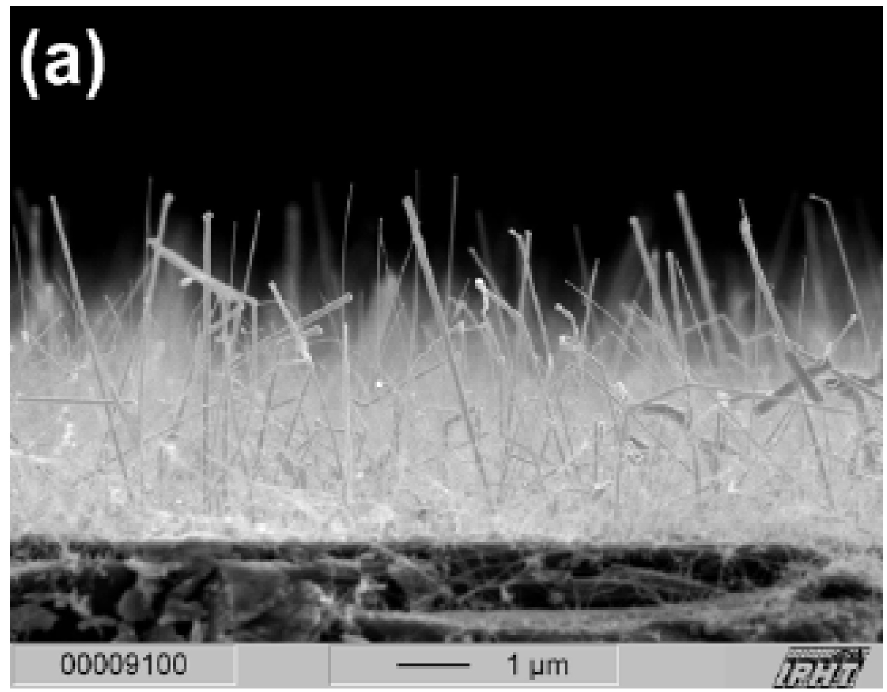
material is removed to provide required form



SiNW arrays by metal assisted wet etching
(N. Petkov et al, Tyndall)

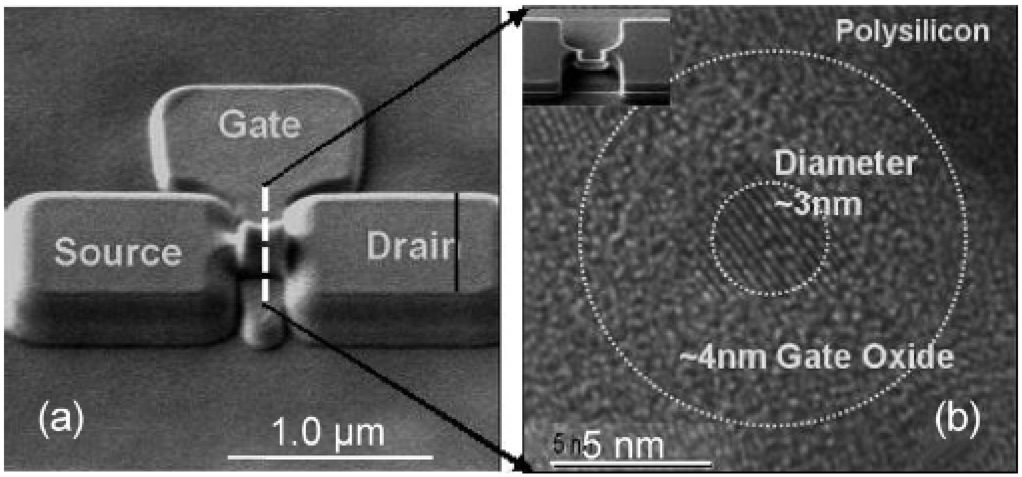
“Bottom-up”

material is synthesised atom-by-atom from



SiNW arrays by VLS growth
(Th. Stelzner et al, IPHT)

Nanowire electronics realisations:
state-of-the-art

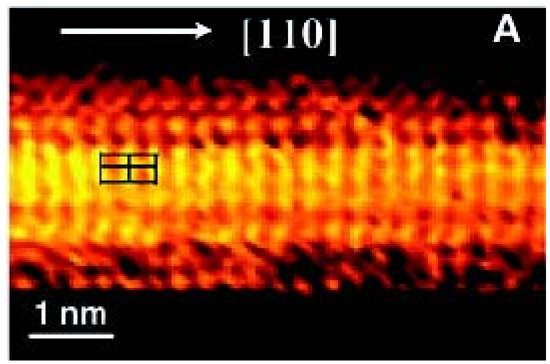


Top-down

Sing *et al*, IEEE TED **55**, 3107 (2008)

Bottom-up

Ma *et al*, Science **299**, 1876 (2003)



size convergence with atomic-scale modelling

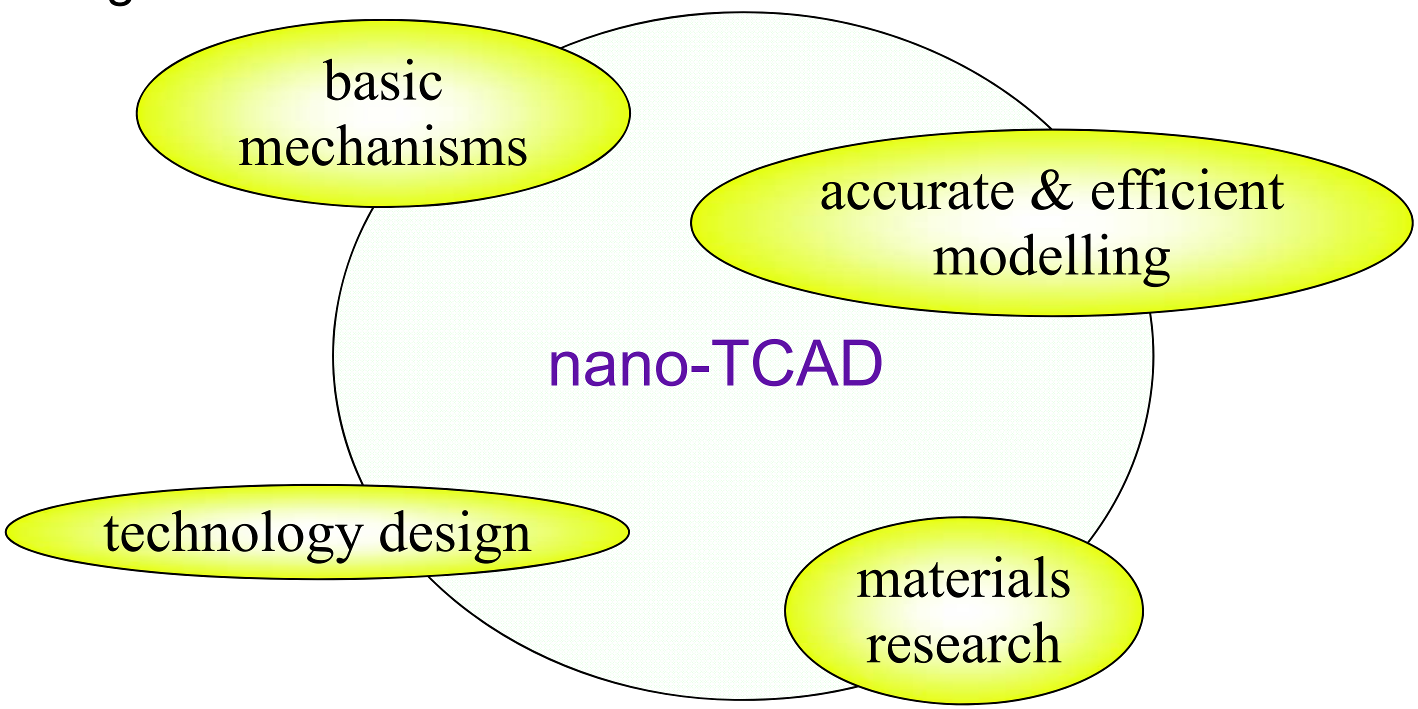
Energy-efficient electronics activity at ETG-Tyndall

primary scientific goals

- nanotechnology-enhanced device operation

specific challenges

- a priori technology evaluation based on atomic-scale description
- device modelling



Simulation framework

Process simulation

Atomic scale growth
Structure determination

Introduction of electrodes

$H_0 + \Sigma_L(\varepsilon) + \Sigma_R(\varepsilon)$

Quantum transport module

Electrical characteristics

Device simulation

Process and device modelling on the same footing

A single level of quantum mechanical treatment

Obtained from or based on first-principles

Density Functional Theory (DFT)

Plane wave implementations

- VASP and Quantum Espresso programme package
  [http://cms.mpi.univie.ac.at/vasp/, http://www.quantum-espresso.org/]
- plane wave basis with 400 eV energy cutoff
- various functionals (LDA, GGA-PBE)
- full relaxation with no symmetry constraints (force < 0.01eV/Å)

Numerical atomic orbital implementations

- OpenMX [http://www.openmx-square.org/]

Density Functional Tight Binding (DFTB)

- approximation for energy functional around reference atomic density
- DFT-parameterised LCAO with minimal basis set for valence orbitals

Th. Frauenheim, G. Seifert, M. Elstner et al, Phys. Stat. Sol. (b) **217**, 41 (2000)

Quantum transport methodology

Current expressed within the Landauer approach

$$i(E) = e/h \times T(E,V)[f_l(E) - f_R(E)]$$

$$I = \int i(E)dE$$

Transmission calculated using the in-house code TIMES (Transport In MEsoscopic Systems)

Scattering matrix of an object connected to two ideal wires via recursive Green's function methods

$$(ES - H)\,G = 1$$

Development principles of TIMES transport module

- **Availability:** source code needs to be accessible

- **Portability:** decoupled from electronic structure platform as much as possible

- **Reusability:** continuous support/development to user requirements

Scalability from:

available platforms

new transport (parallel) algorithms

TIMES Capabilities

Robust generic scientific tool

GF et al, Phys. Rev. B **60**, 6459 (1999) (heat transfer at interfaces and disordered media)
GF, G. Cuniberti, and K. Richter, Phys. Rev. B **63**, 045416 (2001) (molecular electronics with extended Hueckel)
R. Gutierrez et al, Phys. Rev. B **65**, 113410 (2002); GF, A. Kambili, and M. Elstner Chem. Phys. Lett. **389**, 268 (2004) (molecular electronics with methods based on first-principles)
GF et al, Phys. Rev. B **71**, 224510 (2005) (mesoscopic proximity effect with effective mass equations)

Developed to a technology design tool

intel Leap ahead

- modular interface for new applications/electronic structure platforms required

DFTB, Quantum Espresso (Wannier post processing), OpenMX

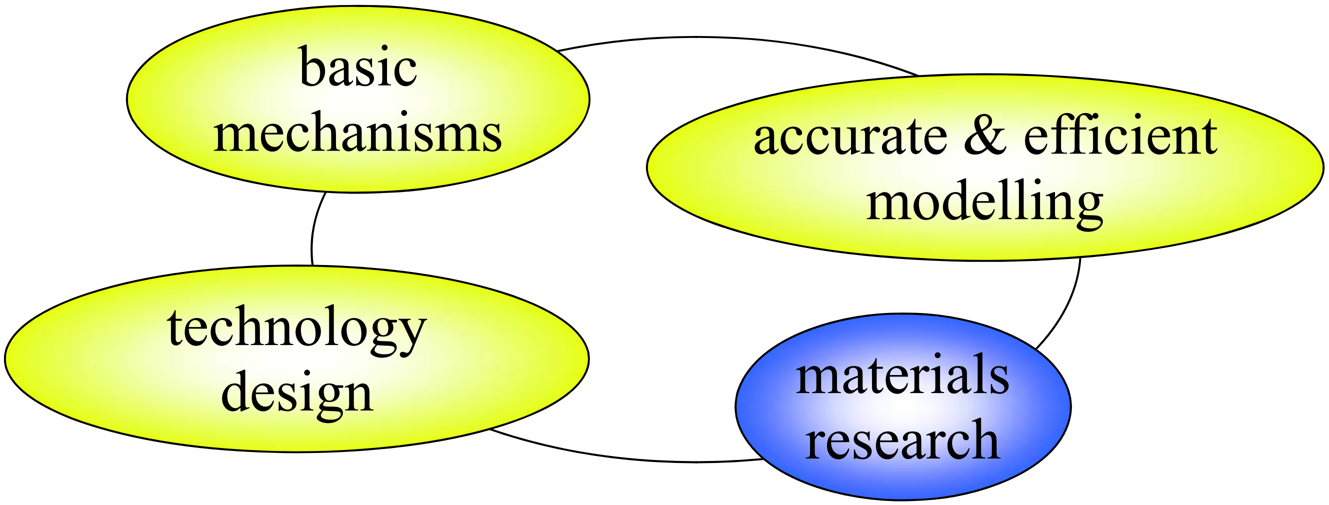
- new parallel algorithms needed

Energy/k-point parallelisation; matrix manipulation in progress

- application-dependent functionalities to be added

Self-consistent charge, gating; inelastic scattering

Open to discuss evaluation and further developments



Background

Methodology

Results

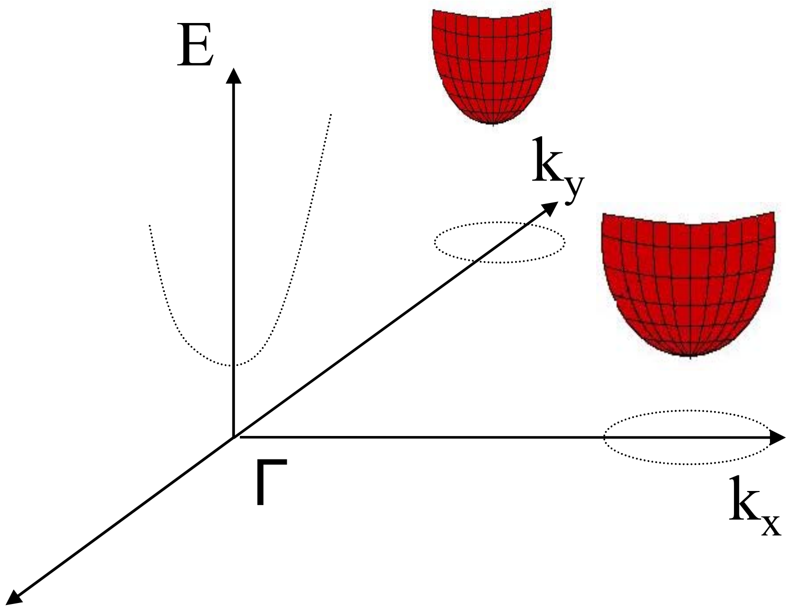
- Band gap modification due to surface termination

Concluding Remarks

Quantum confinement effect

a simple model for Si

A.J. Read et al, Phys. Rev. Lett. **69**, 1232 (1992)



conduction band quantisation (particle in a box)

$$[100]: E_c = E_{c0} + \frac{\hbar^2}{2m_T^*}\left(\frac{n_y\pi}{D}\right)^2 + \frac{\hbar^2}{2m_T^*}\left(\frac{n_z\pi}{D}\right)^2$$

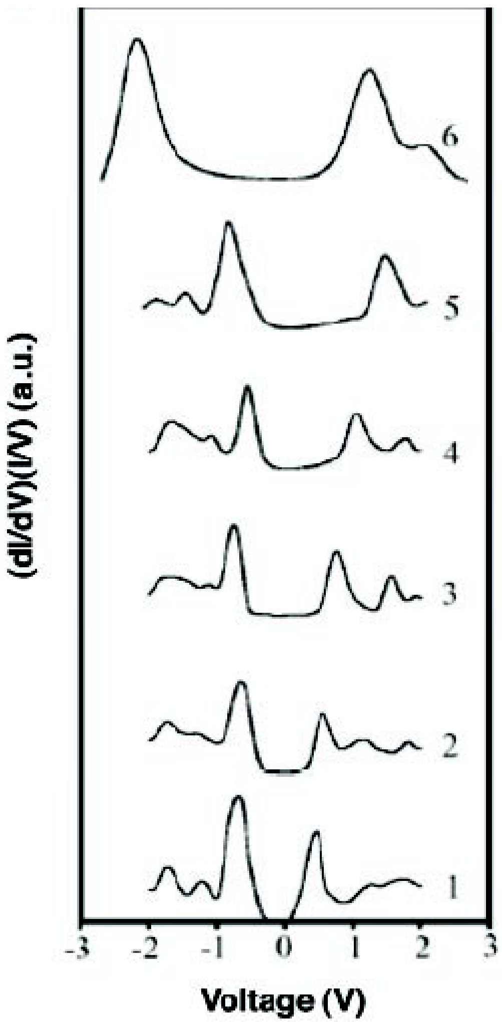
$$[010]: E_c = E_{c0} + \frac{\hbar^2}{2m_L^*}\left(\frac{n_y\pi}{D}\right)^2 + \frac{\hbar^2}{2m_T^*}\left(\frac{n_z\pi}{D}\right)^2$$

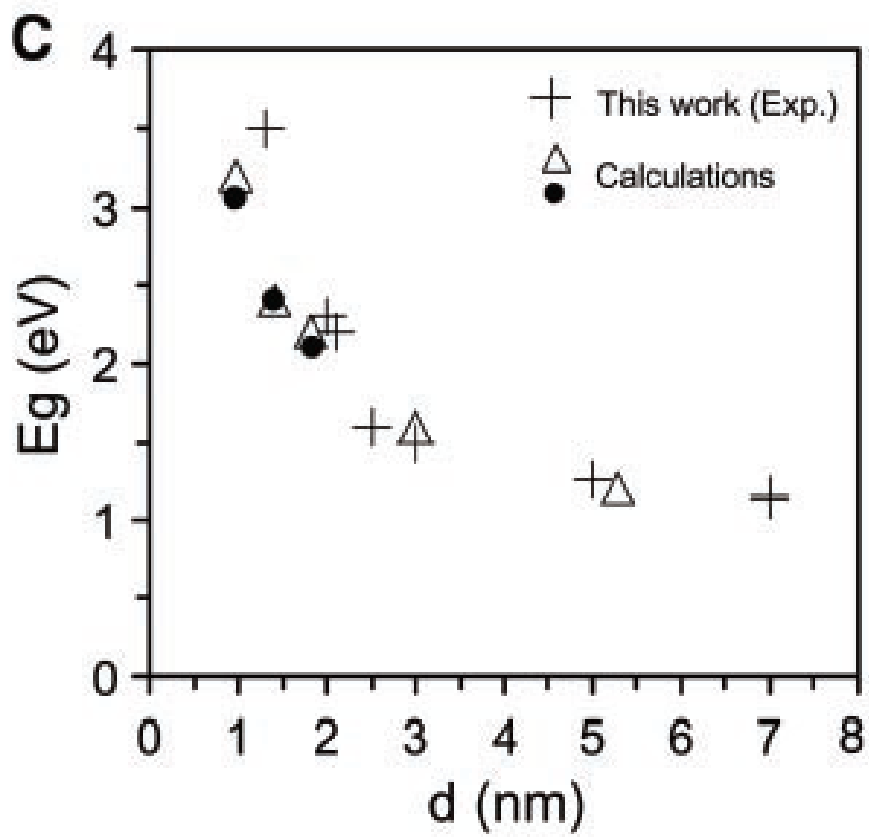
for $n_y = n_z = 1$,
zone folding and $m^*_L > m^*_T$ yields
→ Direct band gap E_g

Similarly for valence band with $m^*_{hh} > m^*_{lh}$; Subtraction of subband energies yields
→ Increasing magnitude of band gap with decreasing diameter

$$\Delta E = \frac{1}{2}\left(\frac{2}{m^*_{hh}} + \frac{1}{m^*_L} + \frac{1}{m^*_T}\right)\left(\frac{\hbar\pi}{D}\right)^2$$

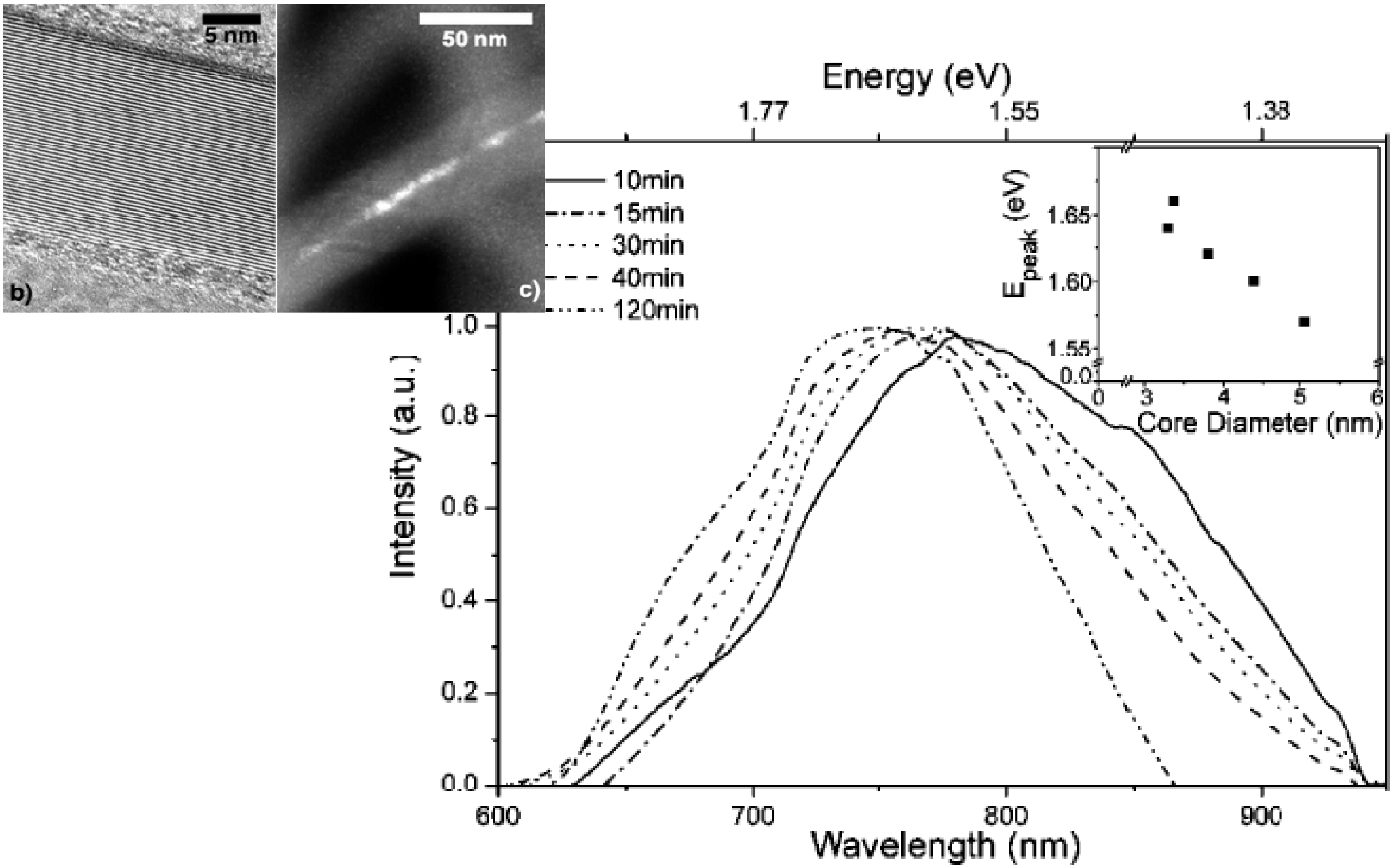
Scanning Tunnelling Spectroscopy





Ma *et al*, Science **299**, 1876 (2003)

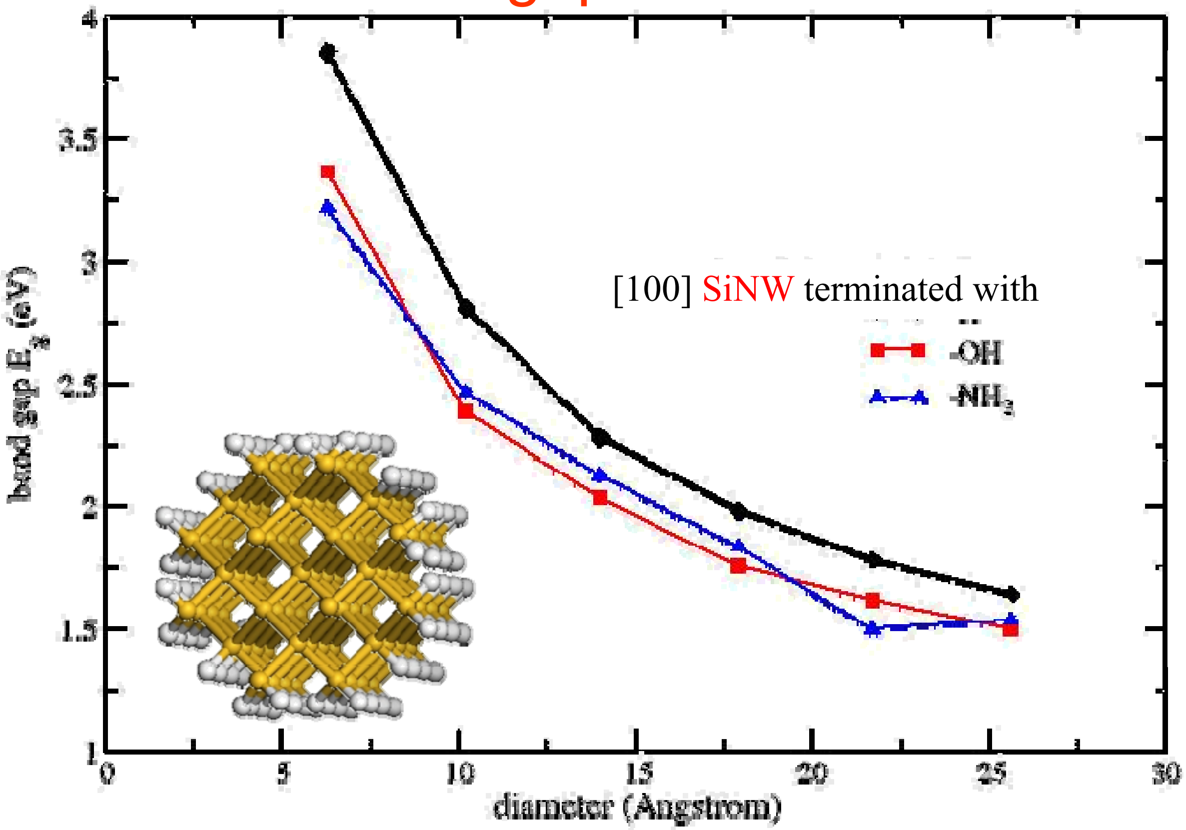
Tunable Light Emission from Quantum-Confinement in Silicon Nanowires



A. R. Guichard *et al*, Nano Lett. **6**, 2140 (2006)

Surface chemistry effects

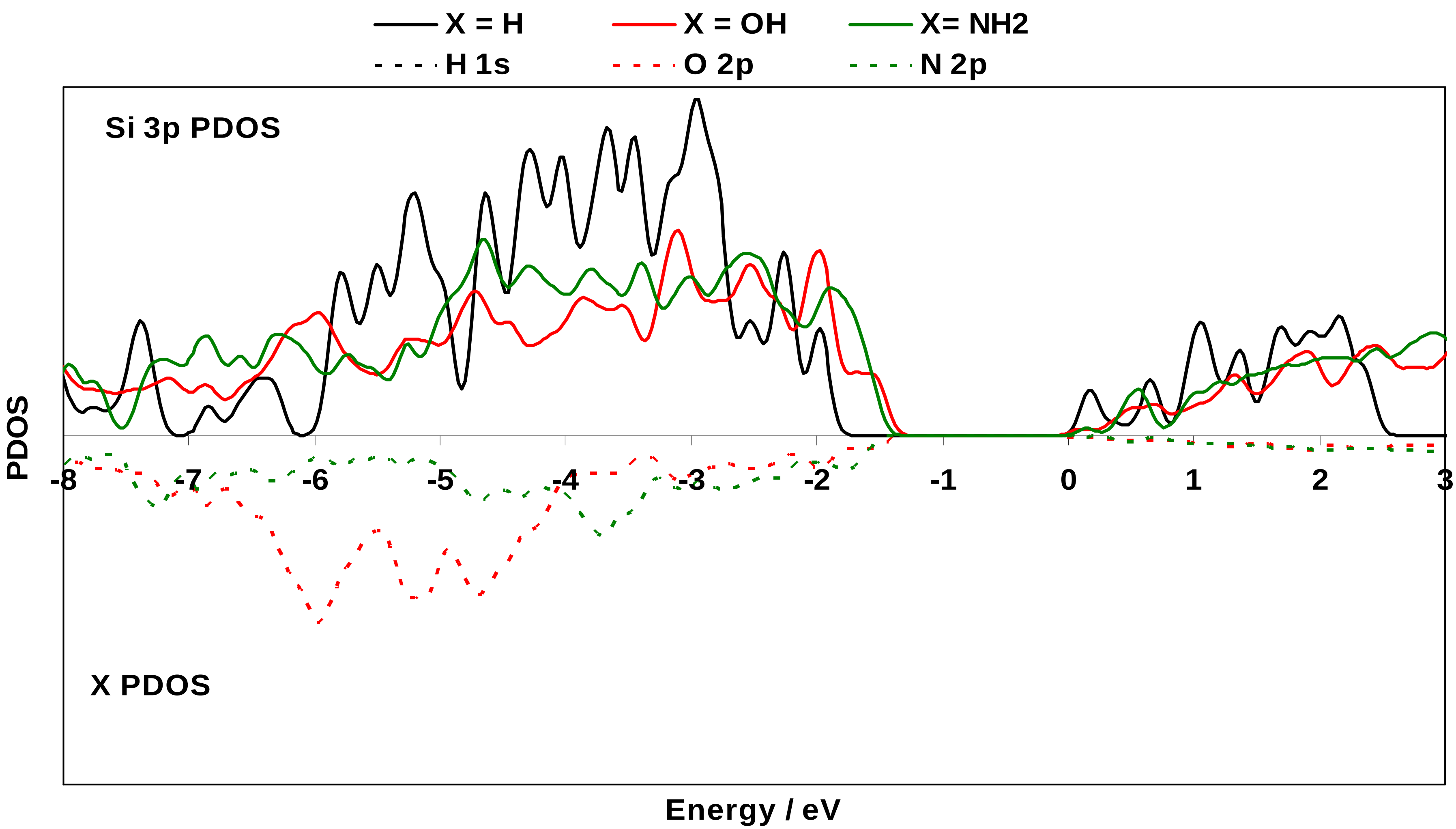
Band gap modification



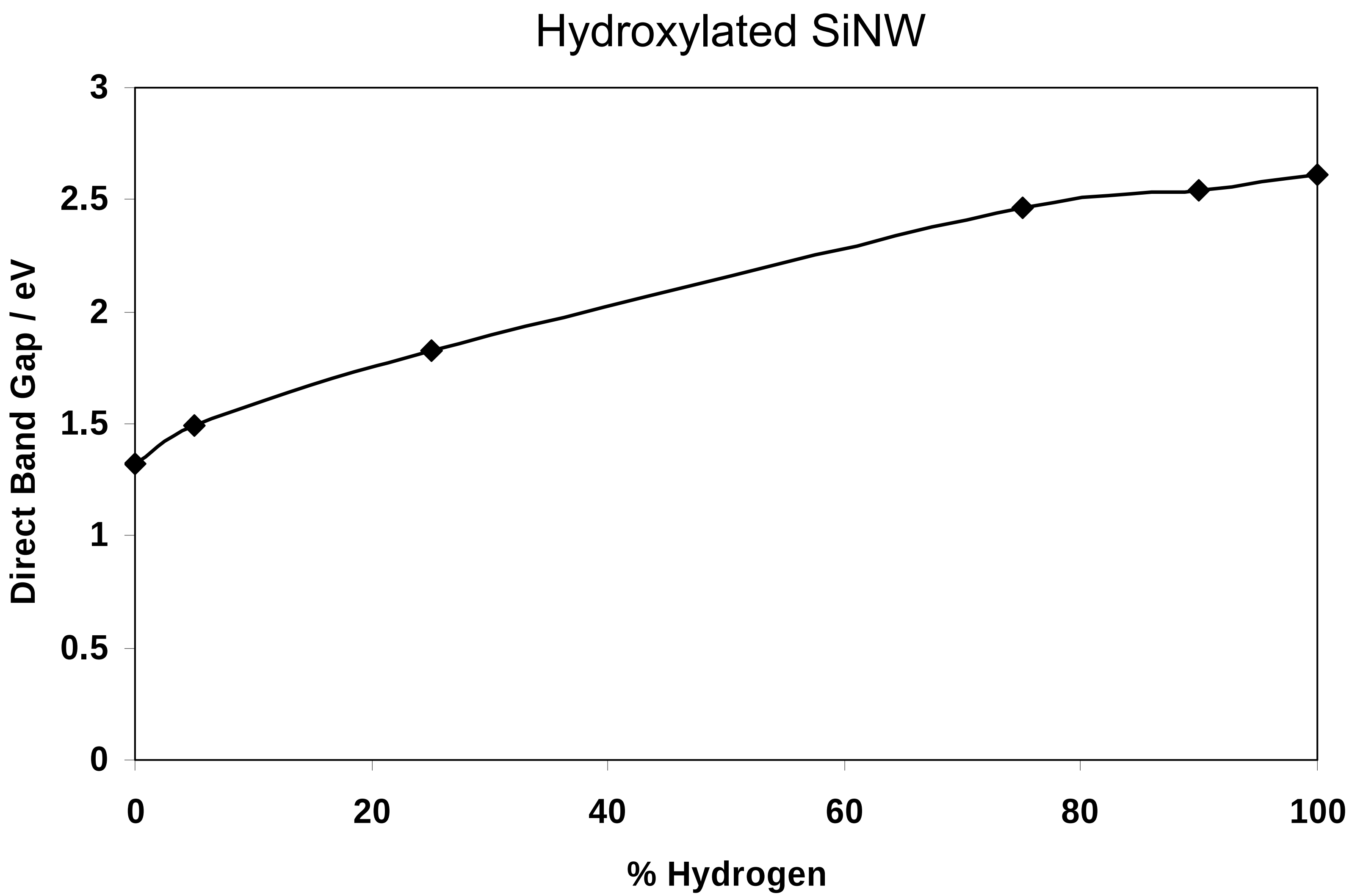
M. Nolan, S. O'Callaghan, G. Fagas, J. C. Greer and Th. Frauenheim, Nano Lett. **7**, 34 (2007)

Hybridisation vs quantum confinement

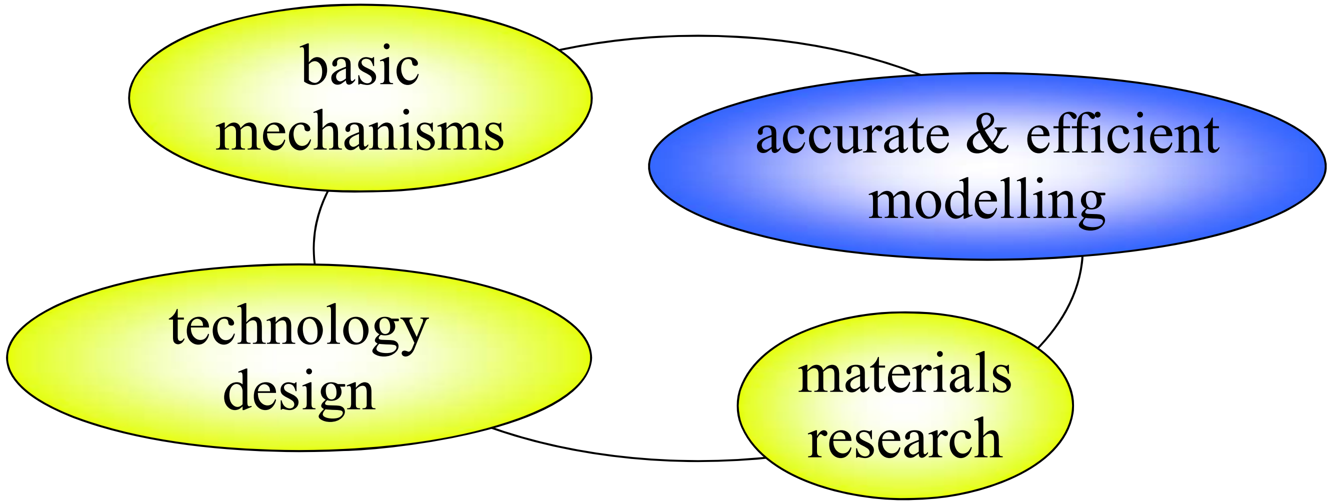
14 Å SiNW (analysis of DFT results)



Tuning via varying surface treatment



Semiconductor Nanowires - Simulations for Technology Design



Background

Methodology

Results

- Computational methods development

Concluding Remarks

Computational challenge

Typical problem: 10^3 nm^3 SiNW (~ 50k Si atoms)

Using minimal basis set of 4 orbitals (s, p_x, p_y, p_z) gives an array of 200000 x 200000

Difficulties → **Turnaround time (beyond my lifetime…)**
Memory footprint (~TByte)

Linear brute-force algorithms:

- **Computational complexity: $O(N^3)$**
- **Memory reqs: $O(N^2)$**

Linear recursive algorithms:

- **Computational complexity: $O(M^3 \times N_x)$; $M = N_y N_z$**
- **Memory reqs: $O(M^2 \times N_x)$**

Parallel algorithms:

- **Computational complexity: $O((M^3 \times N_x)/p + M^3 \times \log_2(D))$**
- **Memory reqs: $O((M^2 \times N_x)/D + M^2 \times D/P)$**

P. S. Drouvelis *et al*, Comp. Phys. **215**, 741 (2006)
S. Cauley et al, J. Appl. Phys. **101**, 123715 (2007)

Nano-TCAD

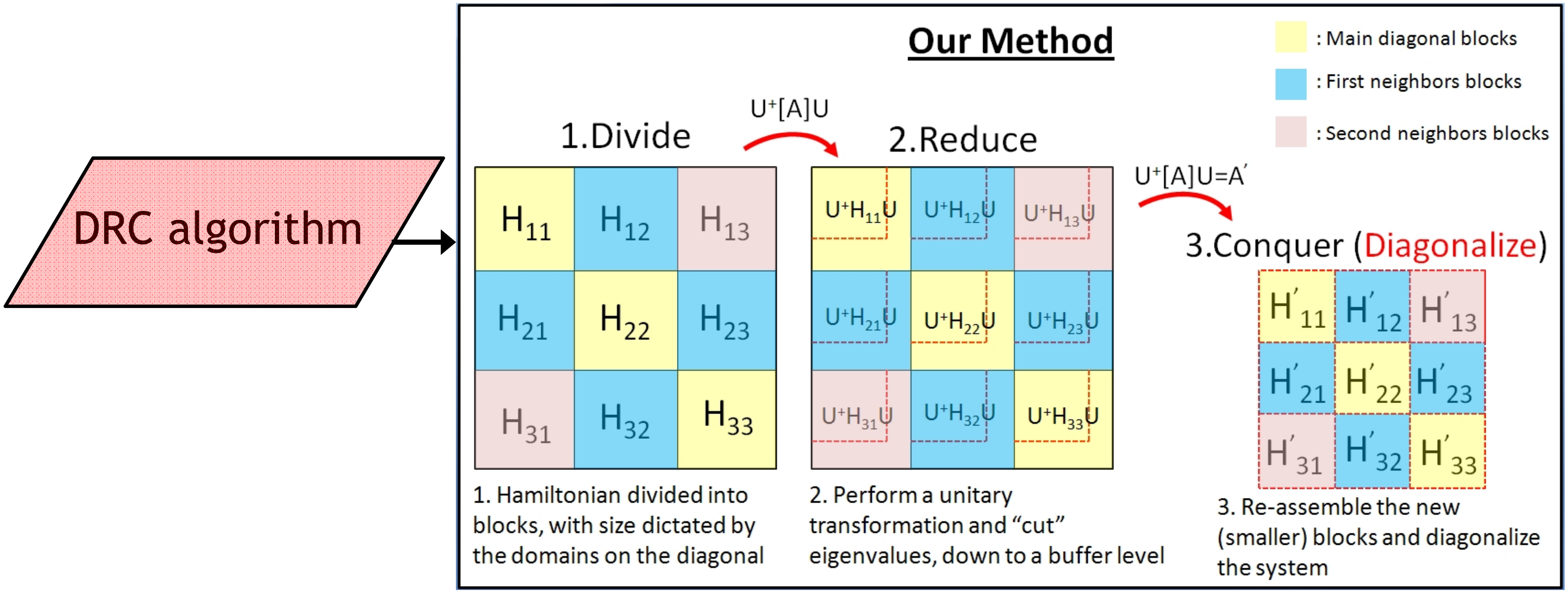
➢ Multiscale/sliding-scale approximation approaches and new parallel algorithms are necessary for technology design based on atomic-scale modelling.

Diagonalisation methods

Common algorithms for computing eigenvalues and their complexity

- **QR algorithm** [O($9N^2$):O(N^3)] (scaling increases with increasing eigenvalue density)
- **Jacobi iterative method** O(N^3) (slower than QR but more accurate and easier to parallelise)
- **Lanczos / Arnoldi iterations** O(N^3) (iterative methods, usage of Krlylov subspace)
- **Divide-and-conquer** [O($N \times log_2 N$):O(N^3)] (dependant on the amount of deflation)
- **SYISDA** O(N^3) (SYmmetric Invariant Subspace Decomposition Algorithm) (mapping the eigenvalues at an [0,1] interval)
- **RRR** O(N^2) / **mRRR** (RELATIVELY ROBUST REPRESENTATIONS) (hybrid of Divide-and-Conquer and inverse iteration)

Divide, Reduce and Conquer (DRC)

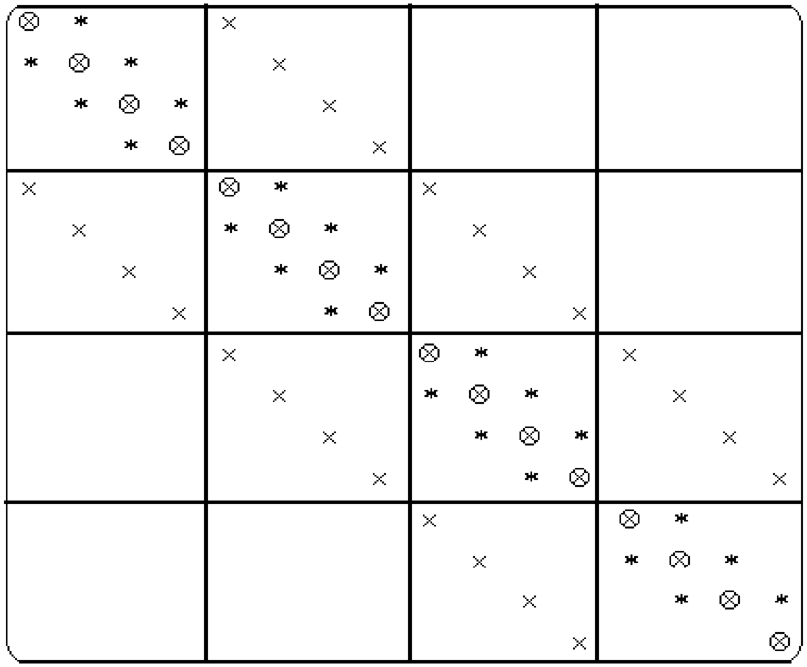


Advantages

- Reduced matrix size
- Inherently parallel development
- Uses a black box for diagonalisation
- Sparse matrices treated in block-tridiagonal as is

(effective mass) model for a nanowire

$H =$



$$\otimes = 2t_x + 2t_y + 2t_z + U_{SC}$$

$$* = 2t_y$$

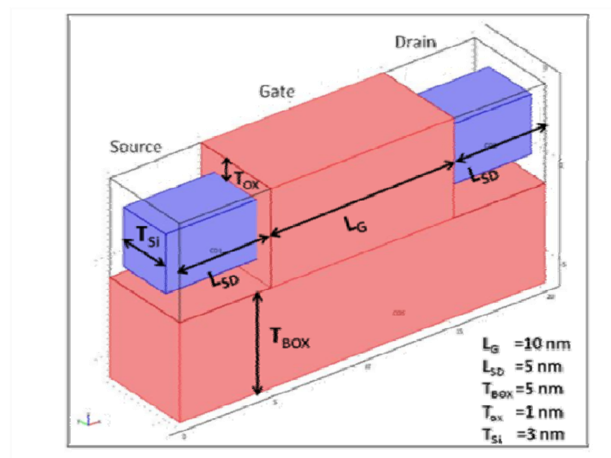
$$\times = 2t_z$$

$$t_{x,y,z} = -\frac{\hbar^2}{2m^*_{x,y,z}}$$

Assume isotropic mass

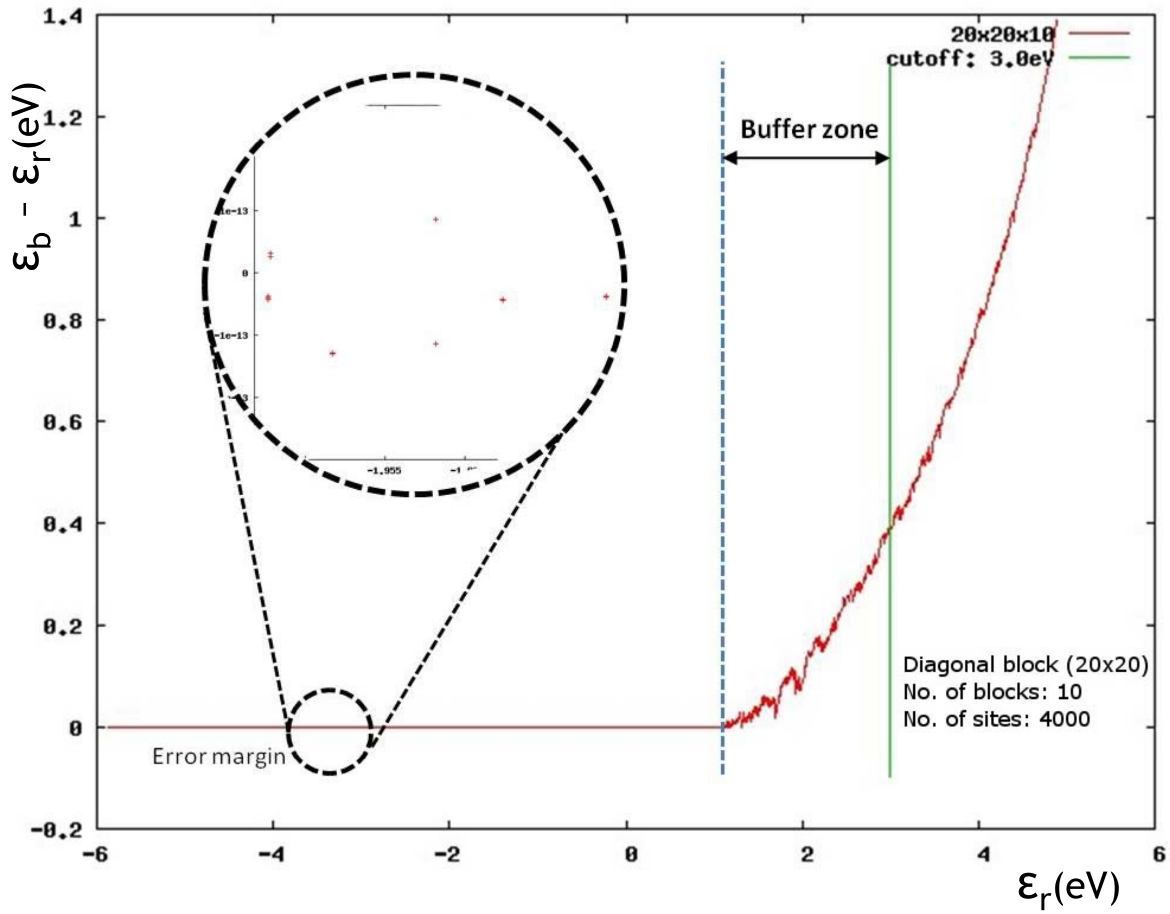
and $U_{SC} = -(2t_x + 2t_y + 2t_z)$

$$\Rightarrow E \in [-6, 6]$$



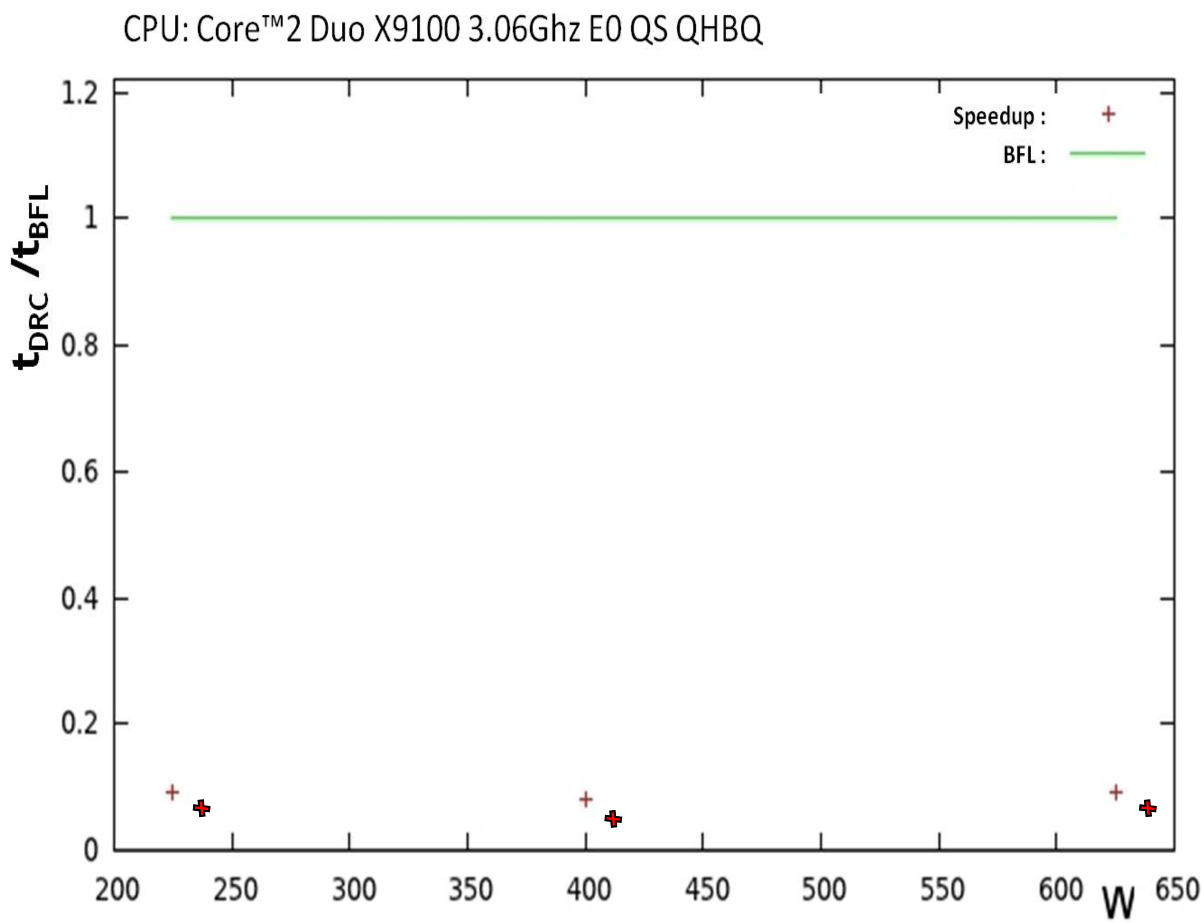
Comparison of DRC against full eigenvalue solver LAPACK for several sizes of model nanowires between 250 to 9000 sites.

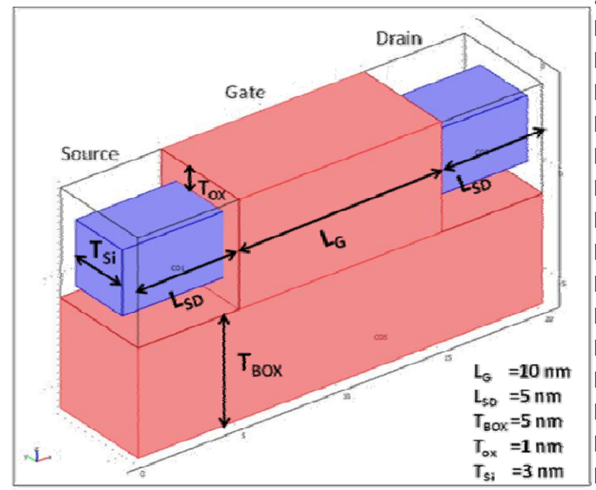
Selected eigenvalues $\varepsilon_c = 3.0eV$

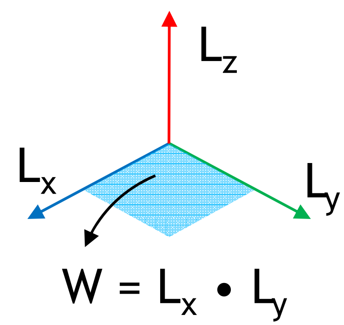


- A buffer zone defines the region between the cutoff energy and the maximum of the desired eigenvalue spectrum
- Below the buffer zone the spectrum is very accurate

Constant length, variable W

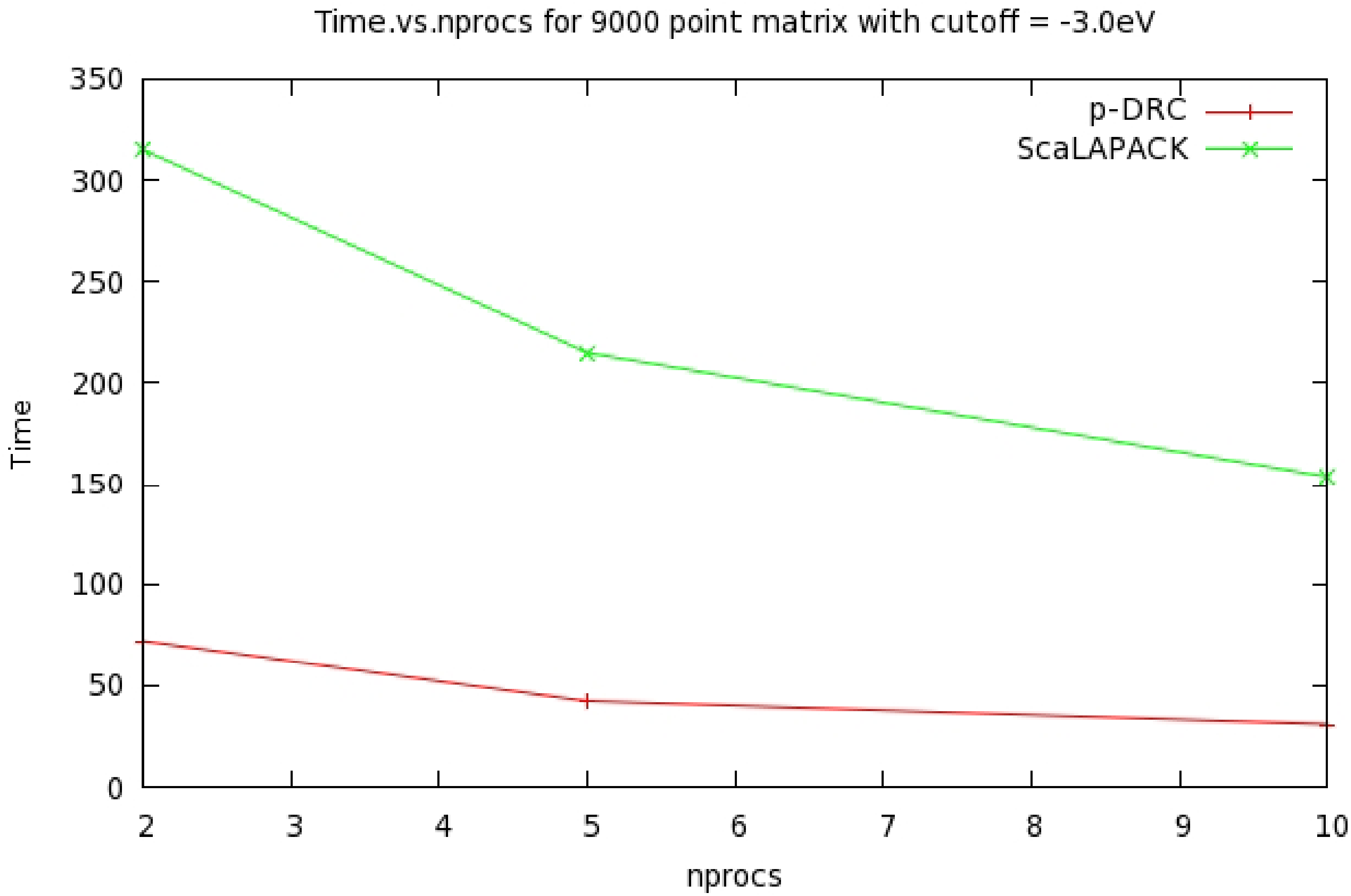






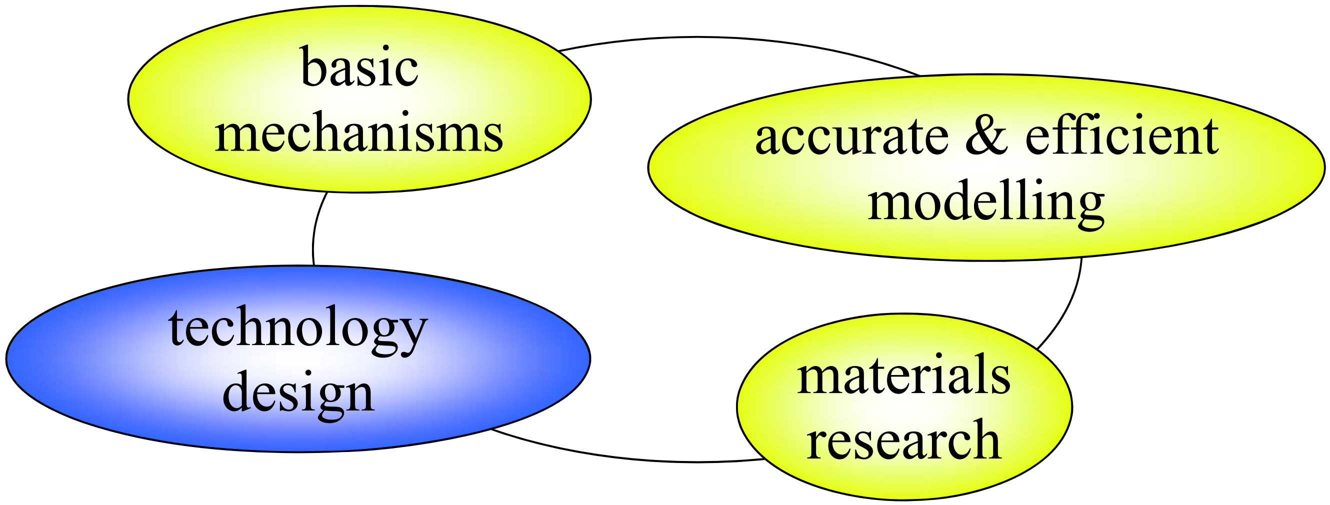
M. Iakovidis and G. Fagas, in preparation

Parallel implementation



M. Iakovidis and G. Fagas, in preparation

Semiconductor Nanowires - Simulations for Technology Design



Background

Methodology

Results

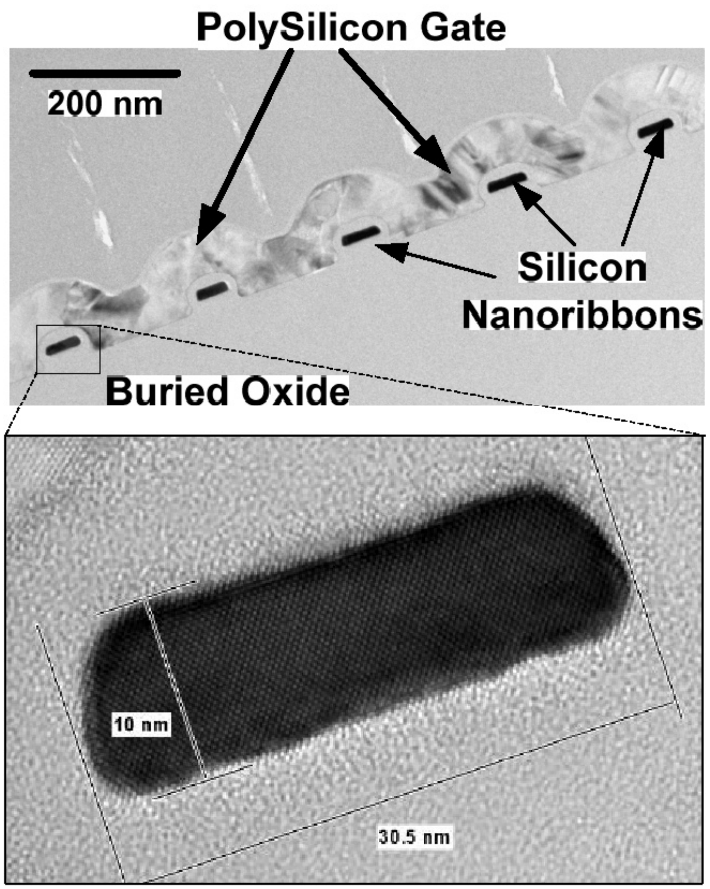
- Nanowire-based CMOS

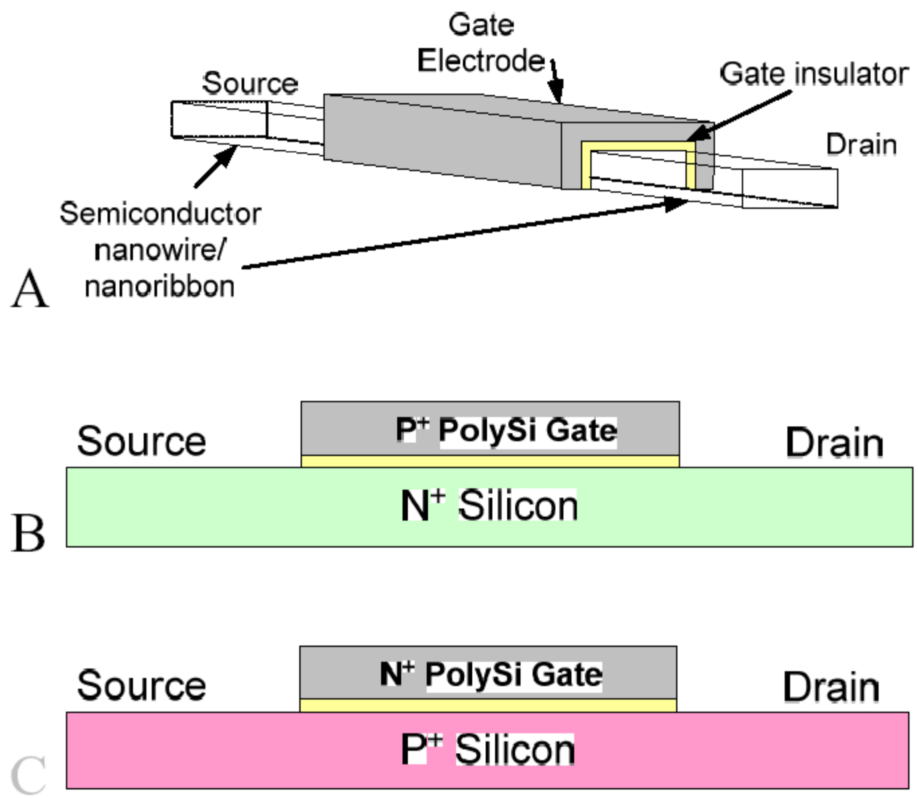
Concluding Remarks

Junctionless transistor

Gated Resistor (or CMOS without junctions) → no doping gradients

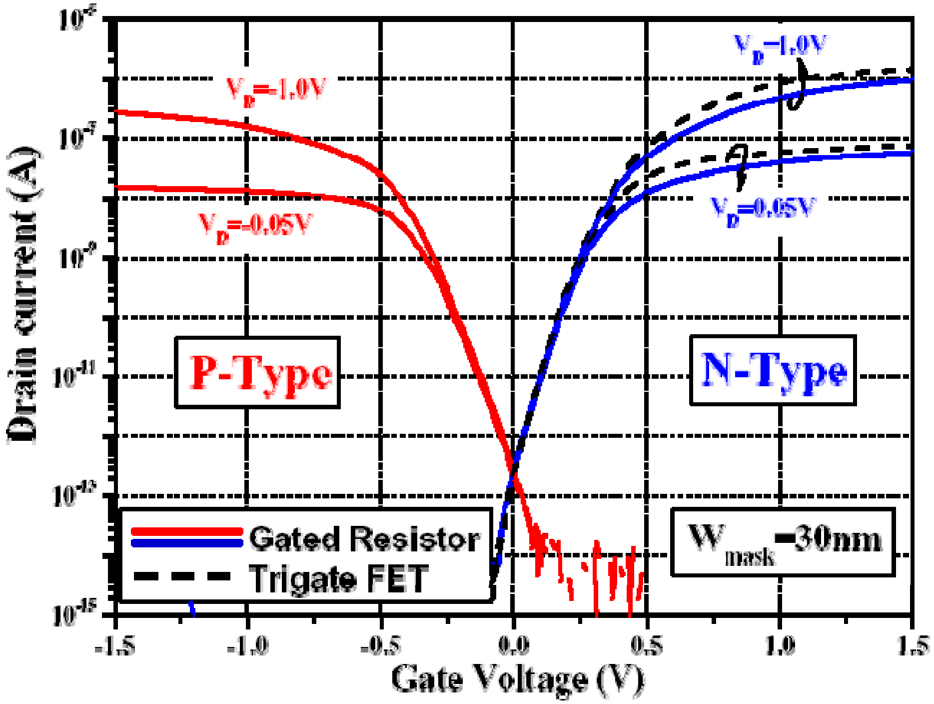
The cross-section of the channel is small enough that gate can deplete the heavily doped channel (8×10^{19} cm^{-3}) entirely, hence can turn off device





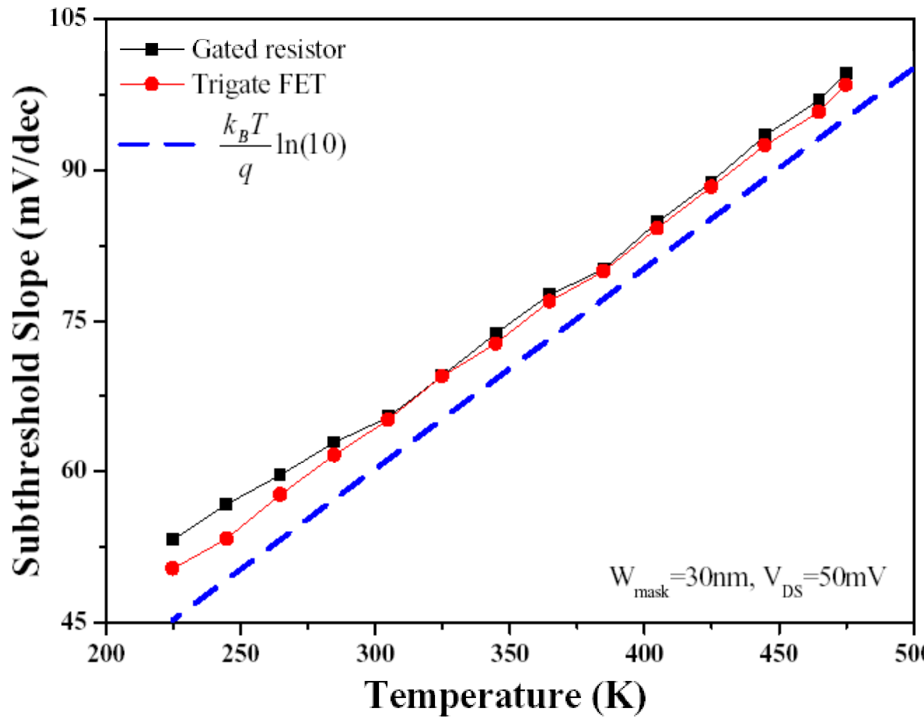
J.-P. Colinge et al, Nat. Nanotech. **5**, 225 (2010)

Junctionless transistor characteristics



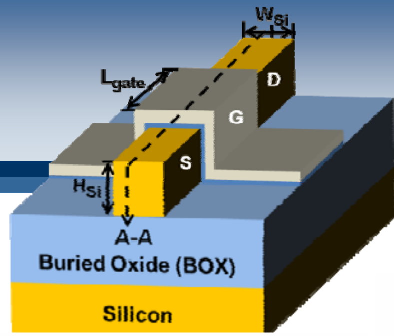
J-.P. Colinge et al, Nat. Nanotech. **5**, 225 (2010)

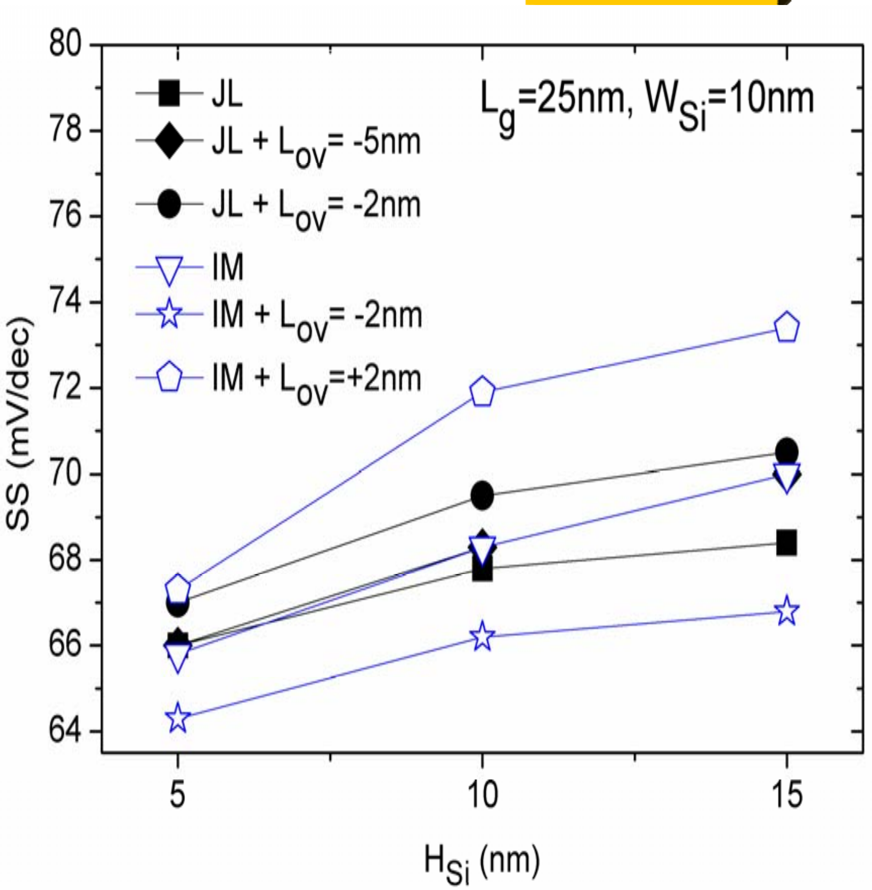
$$SS = \frac{dV_G}{d\ \log\left(I_D\right)}$$

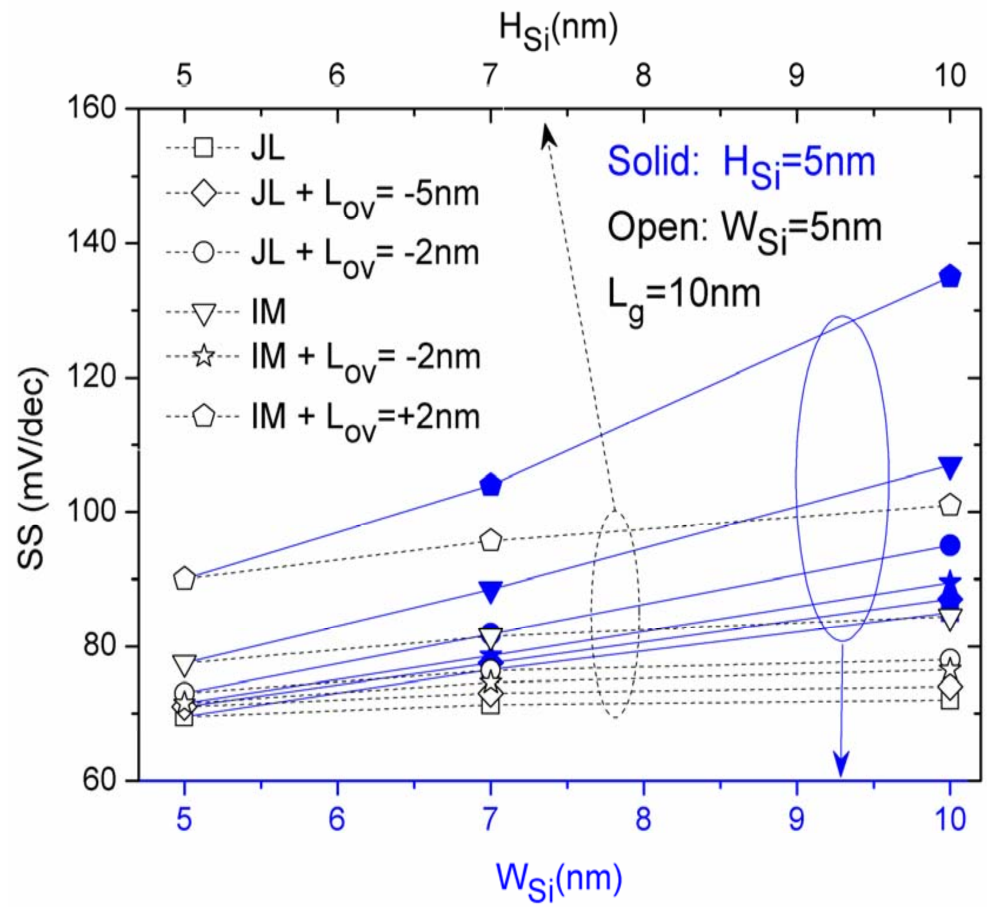


new devices show even smaller short channel effects

Short channel effects
JL and IM comparison



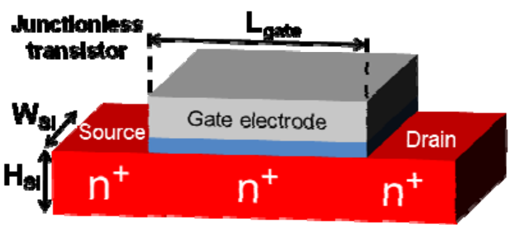




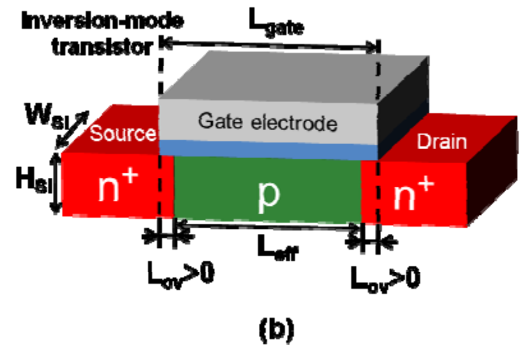
P. Razavi et al, *submitted*
Similar for Accumulation Mode:
P. Razavi et al, DOI 10.1109/ULIS.2011.5758005

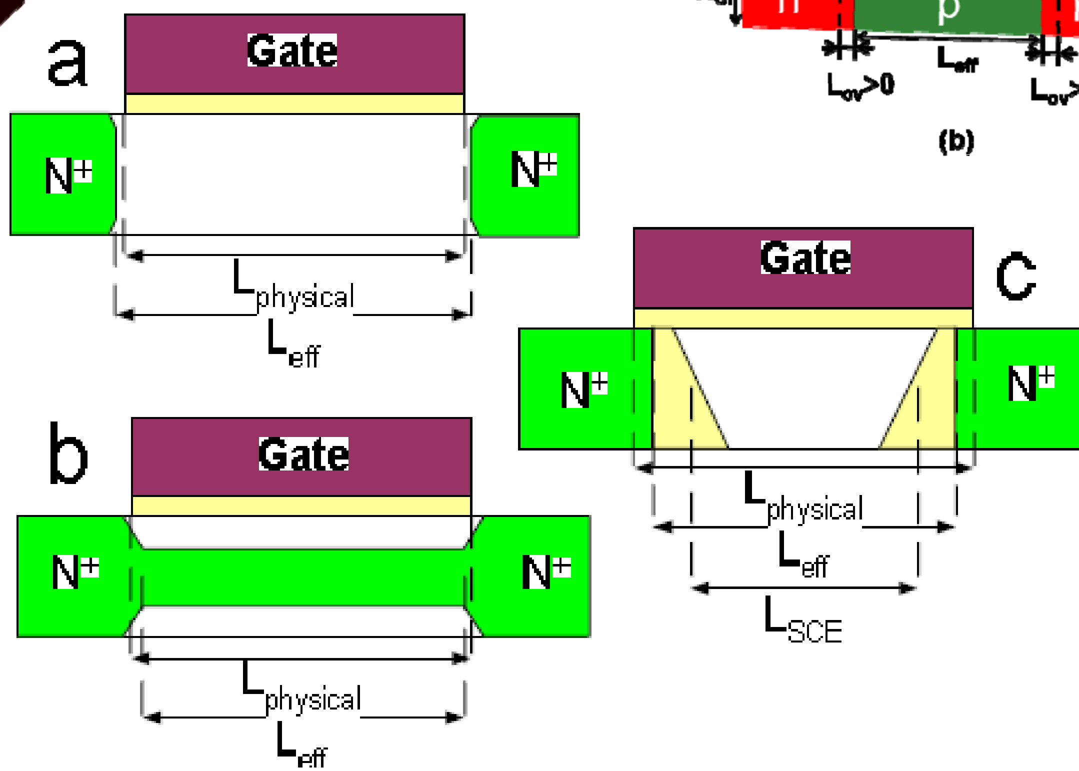
Effective gate length

Junctionless (JL)



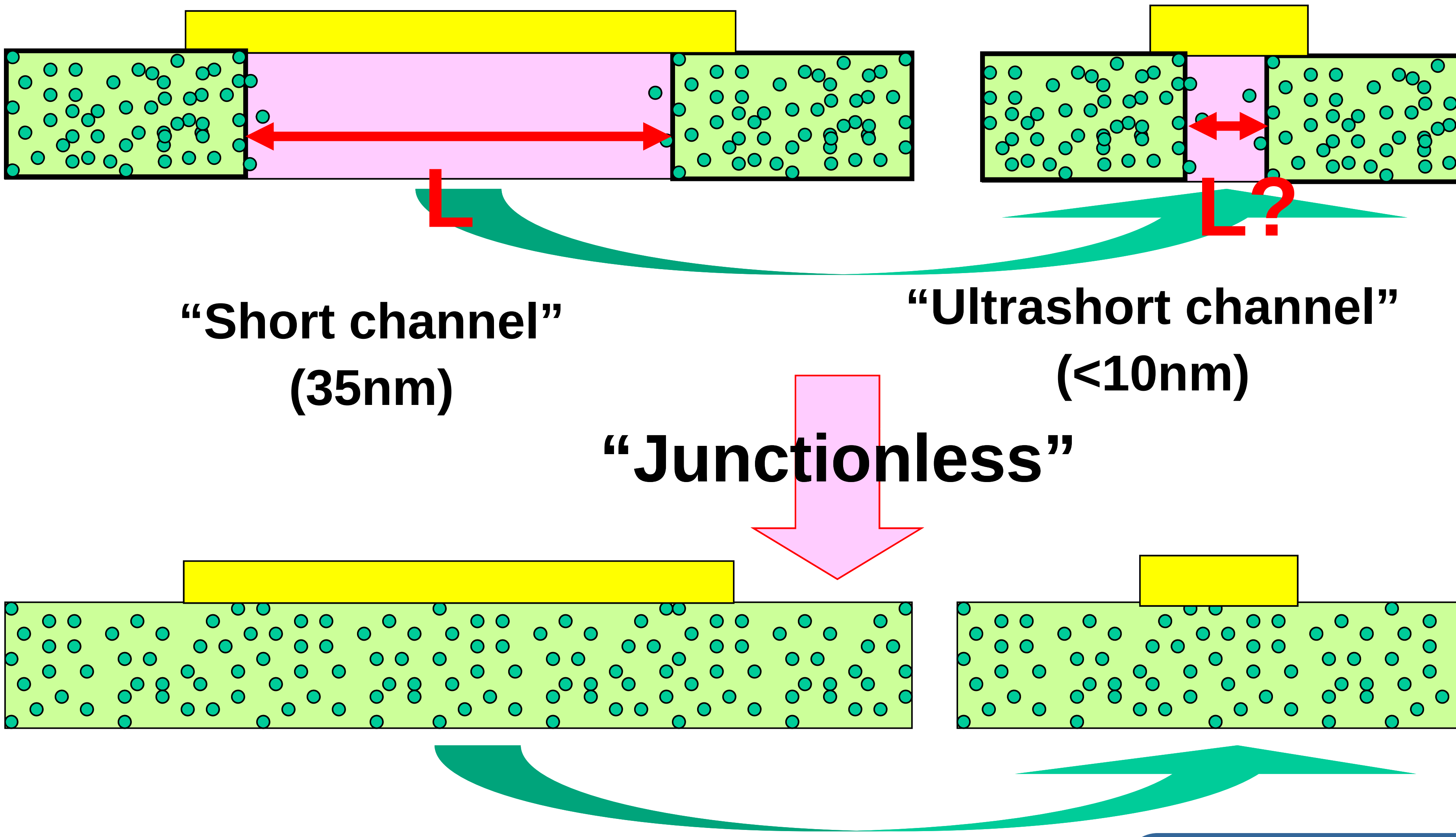
Inversion Mode (IM)





J-.P. Colinge et al (2011)

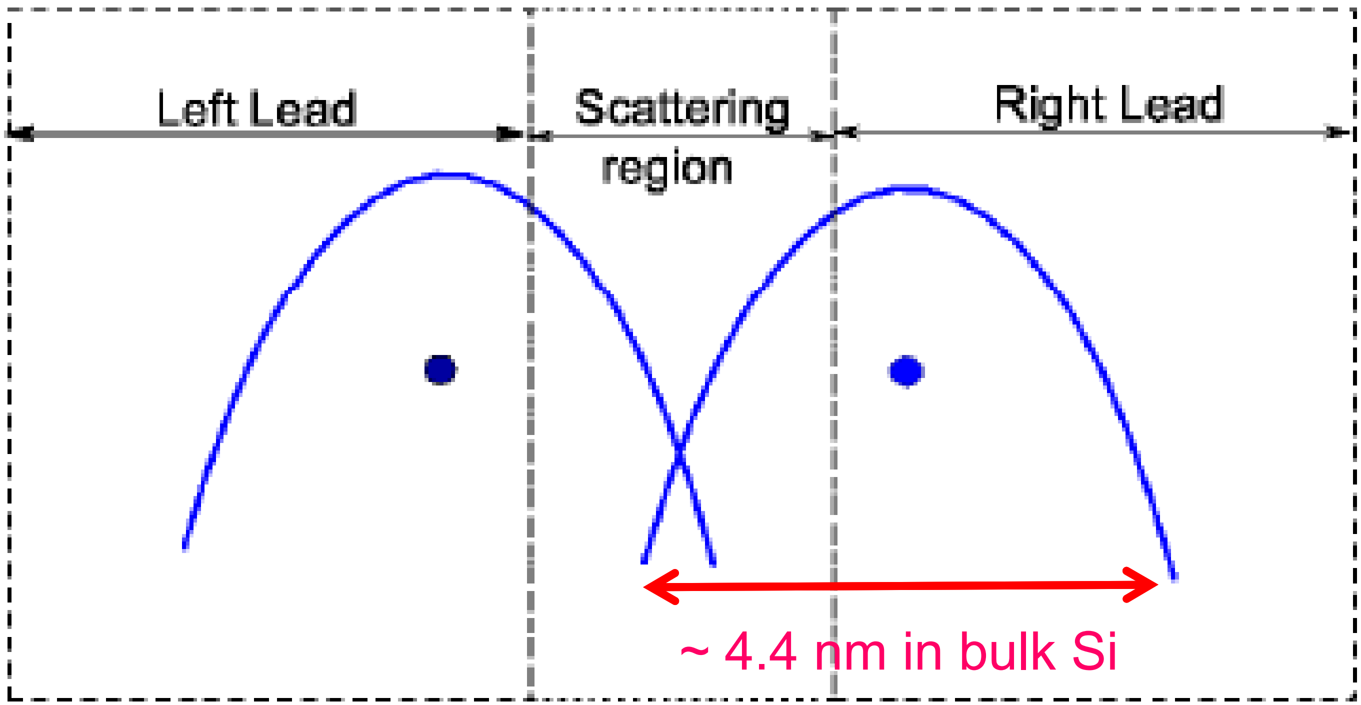
Dopant profile issue



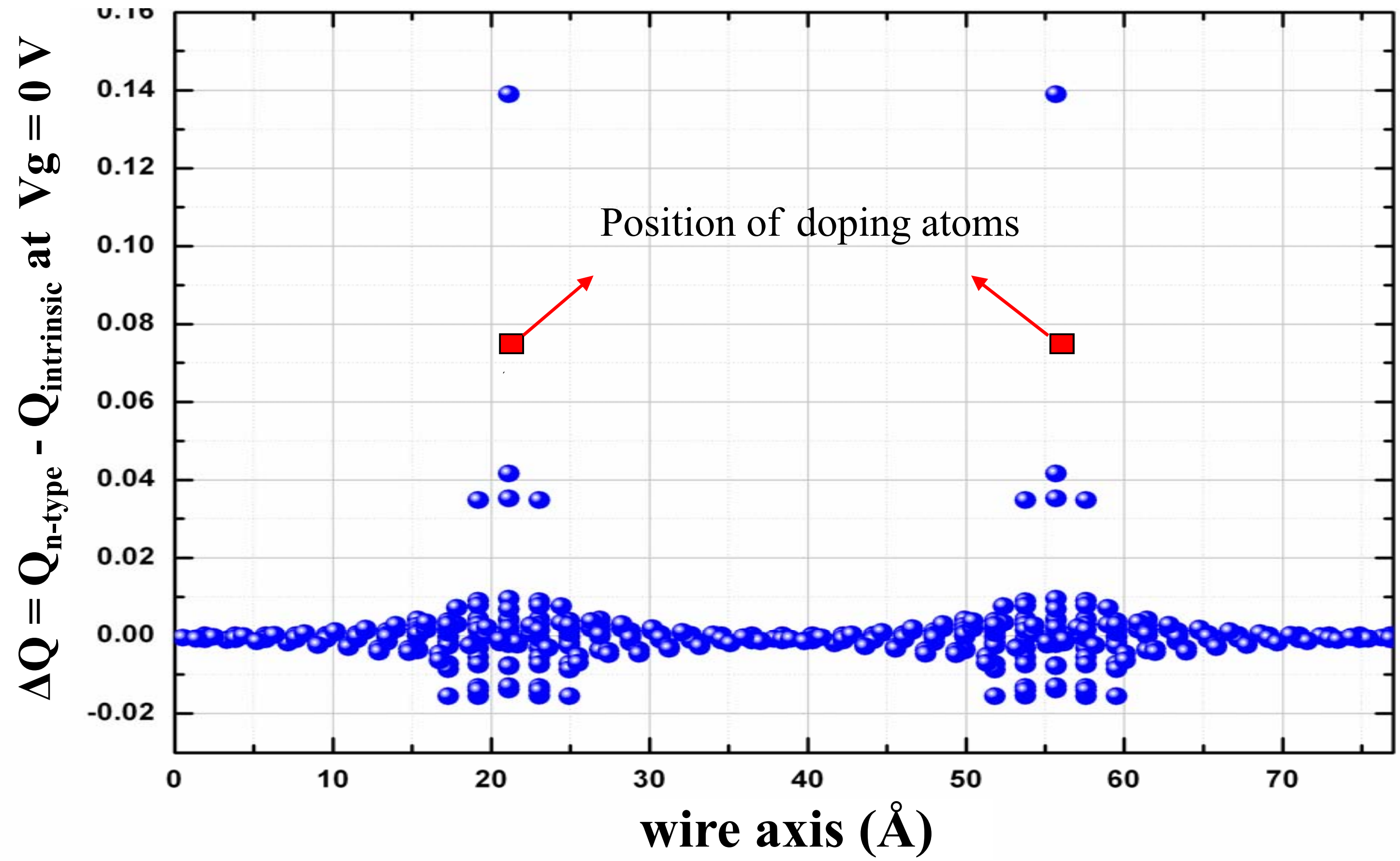
Dopant extension issue

Hydrogenic impurity model

$$E_n \approx -Ry\frac{m^*}{\varepsilon^2}\frac{1}{n^2}, \qquad a_B \approx \left(\varepsilon/m^*\right)a.u. \approx \left(11.4/0.3\right)a.u.$$



Mulliken population



localization radius of the dopant electron or hole is ~ 1.5 nm

L. Ansari, B. Feldman, G. Fagas, J-.P. Colinge, and J. C. Greer,
Appl. Phys. Lett. **97**, 062105 (2010)

- **Classical device simulation**

C.W. Lee *et al*, Appl. Phys. Lett. **94**, 053511 (2009)

- **Experimental device**

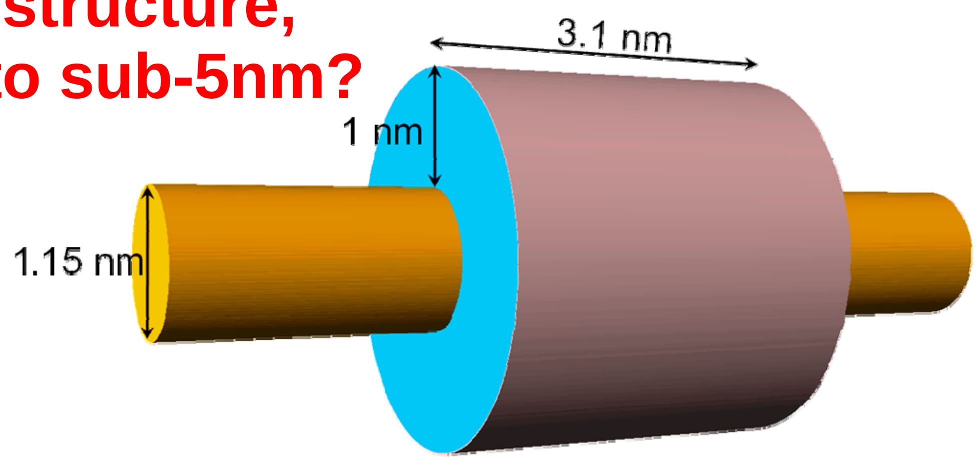
J-.P. Colinge *et al*, Nature Nanotech. **5**, 225 (2010)

- **Geometry dependence in classical and quantum devices**

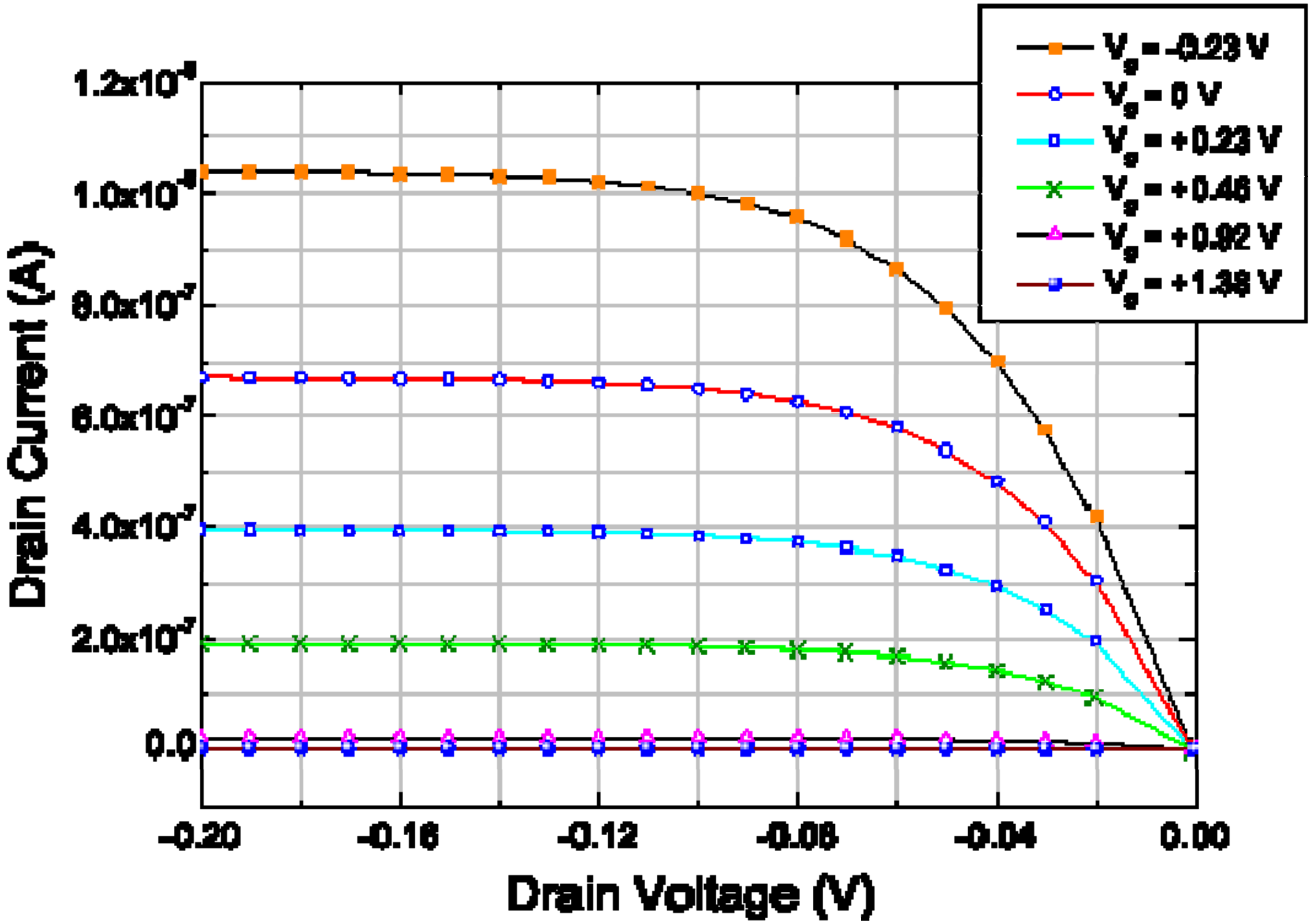
P. Razavi *et al*, *submitted* (2011)

Gate length L_g > 10nm

Using realistic electronic structure, can the device scale down to sub-5nm?



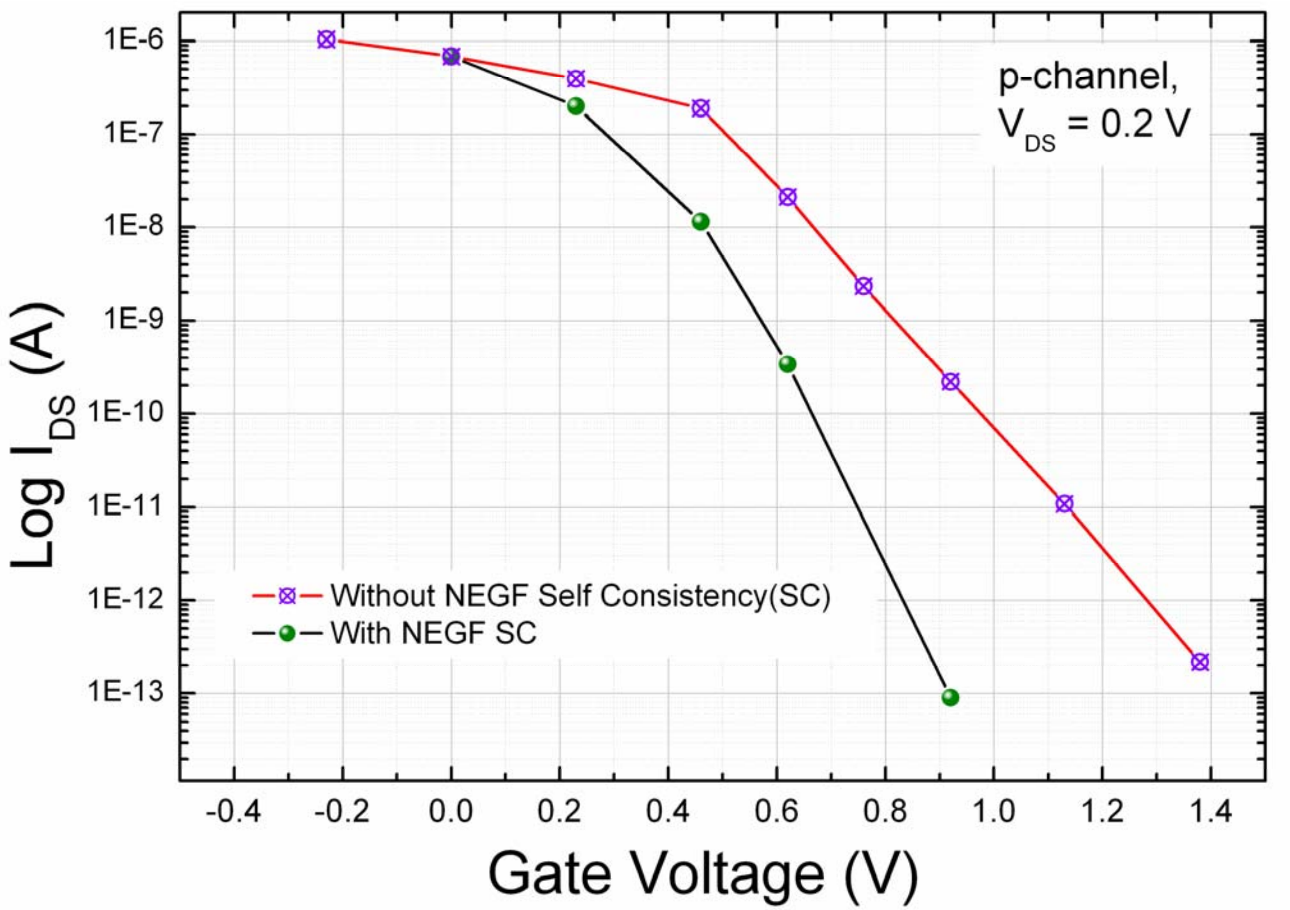
Transistor behaviour at 3nm



p-type (Ga doped)
8 x 10^{20} cm^{-3}

L. Ansari, B. Feldman, G. Fagas, J-.P. Colinge, and J. C. Greer, Appl. Phys. Lett. **97**, 062105 (2010)

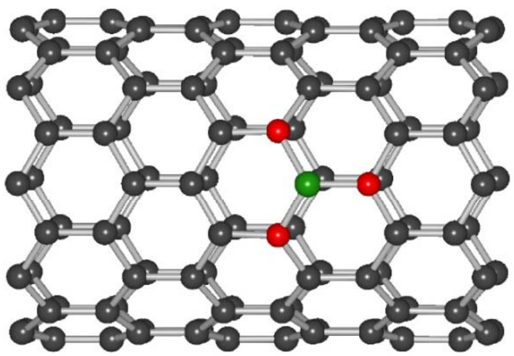
Subthreshold slope



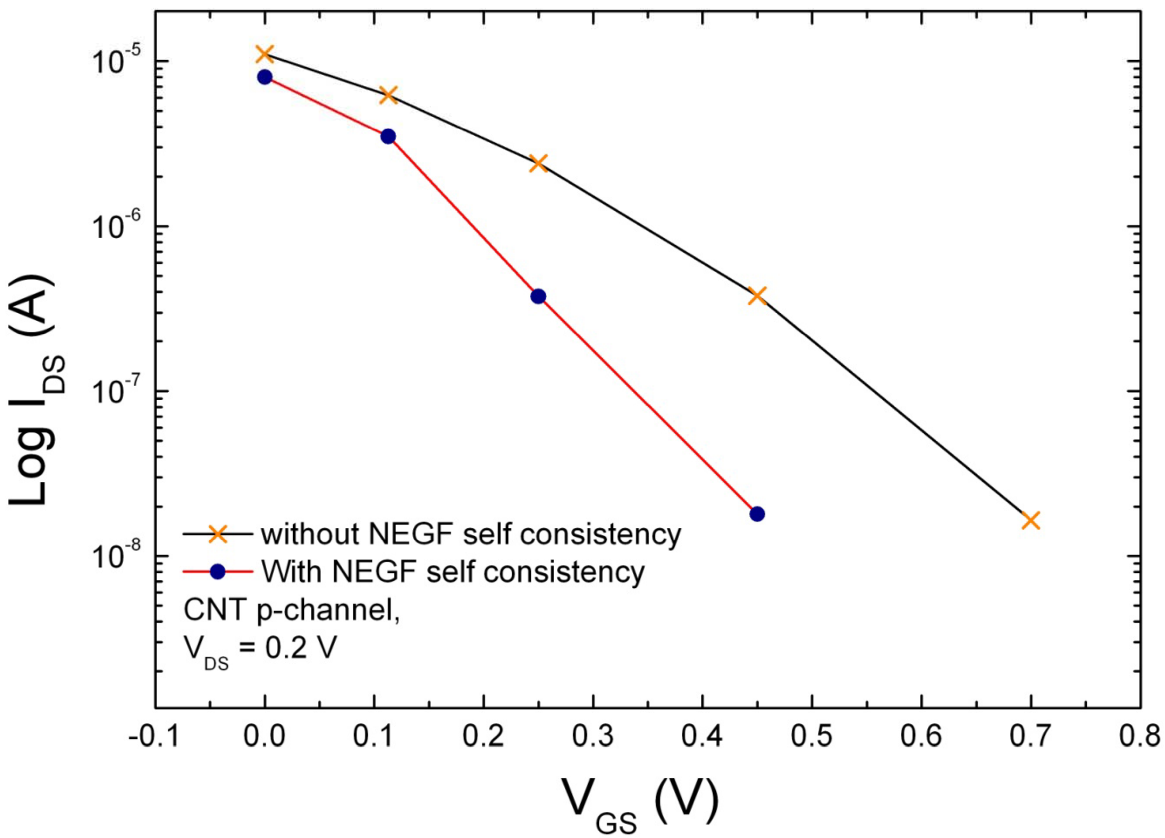
~ 80 mV /decade → near to theoretical limit!

L. Ansari, B. Feldman, G. Fagas, J-.P. Colinge, and J. C. Greer, Sol. Stat. Elec. (2011)

CNT junctionless transistors

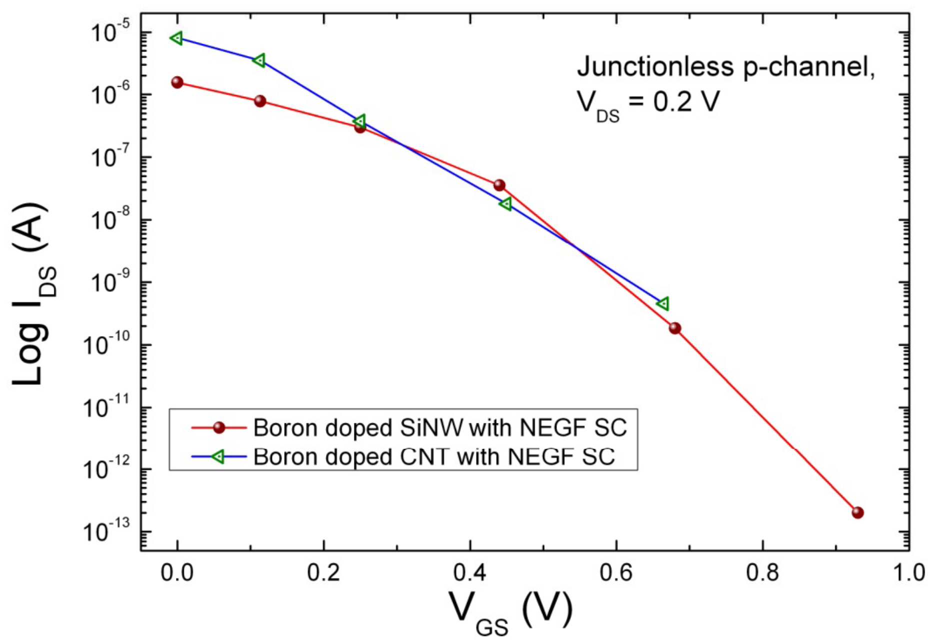


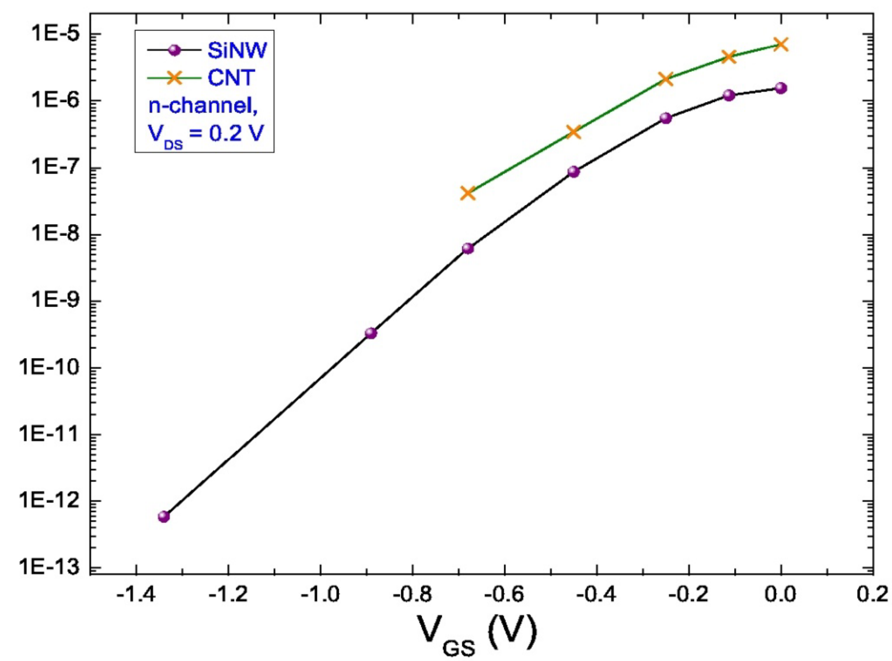
p-type (1.1% B doped)



L. Ansari et al, in preparation

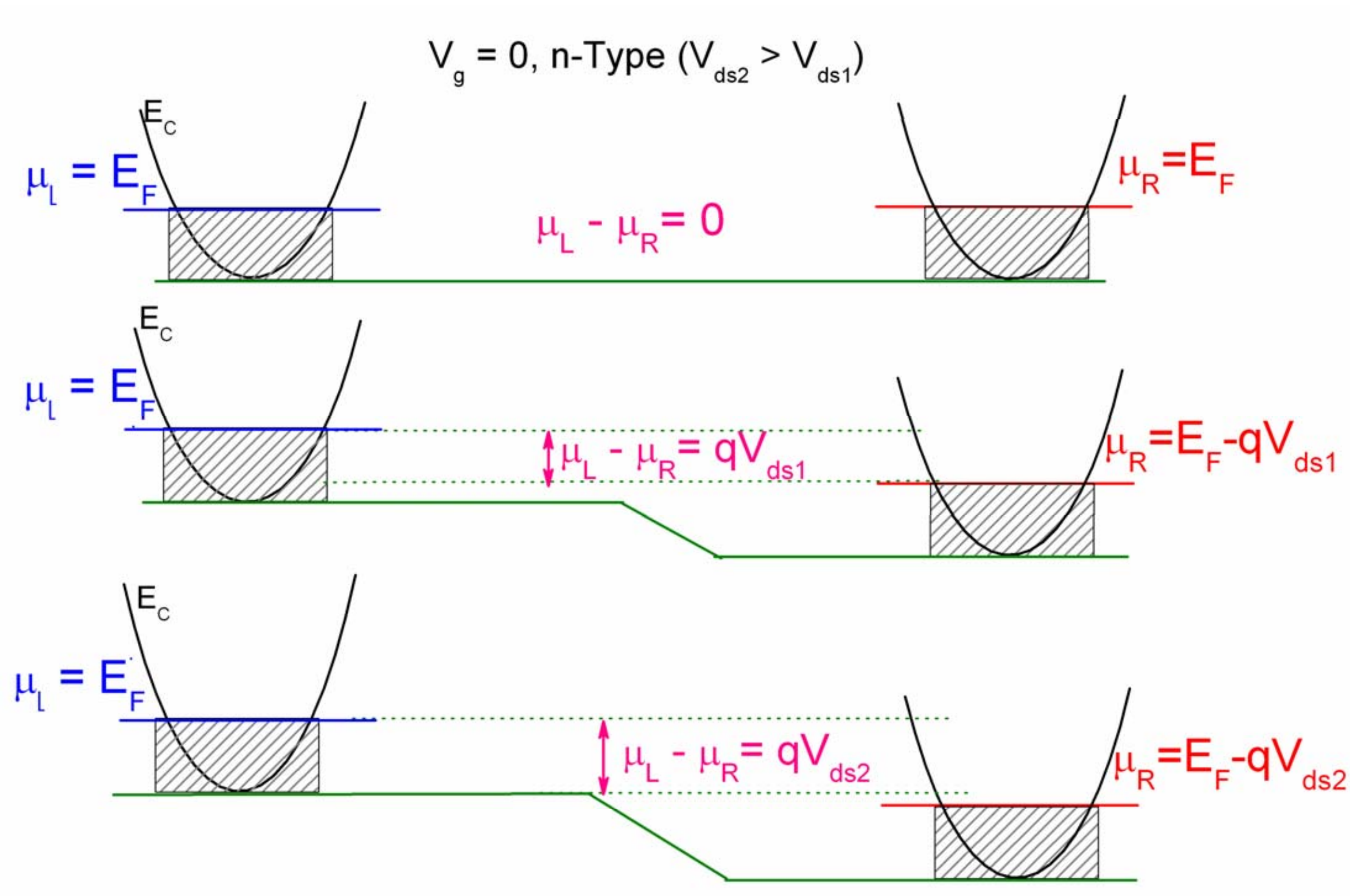
Si and CNT JL transistors comparison



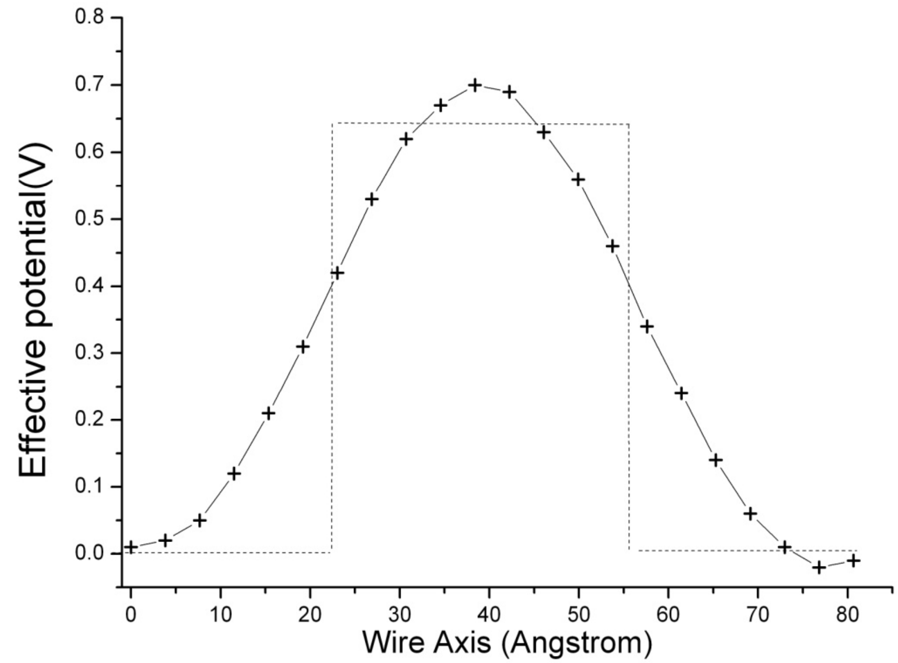


L. Ansari et al, in preparation

Current saturation



Estimates of I_{on} and I_{off}



On-state:

$$I_{on} \approx \frac{2e^2}{h} \times \text{number of channels} \times V_{ds}$$

Off-state:

$$I_{off} \approx \frac{2e^2}{h} \times \text{number of channels} \times T_{WKB} \times V_{ds}$$

$$T_{WKB} = \frac{\exp\left(-2\sqrt{2m^*/\hbar^2 \, eV_b} L_G\right)}{\left[1 + \frac{1}{4}\exp\left(-2\sqrt{2m^*/\hbar^2 \, eV_b} L_G\right)\right]^2}$$

Background

Recent results and methodology

Next steps

Concluding remarks

Summary

- Due to size-effects surface chemistry does influence the electronic structure and, hence, the electrical and optical properties

- Reduced scattering in [110] nanowires compared to [100] nanowires

- Conventional p-n junctions cannot be routinely formed at the few nanometer length scale and the junctionless transistor design offers a viable alternative

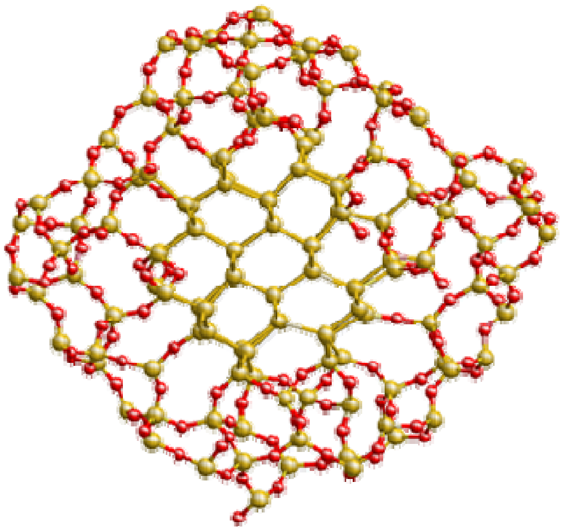
- Multiscale/sliding-scale approximation approaches and new parallel algorithms are necessary for technology design based on atomic-scale modelling → Divide, Reduce and Conquer

Summary

➢ Semiconductor nanowires provide an ideal technology enabling platform

Several open issues regarding:

- surface chemistry
- realistic interfaces
- doping and dopant level fluctuations
- energy dissipation due to e-ph coupling



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Thank you!

Q&A