Microenergie e ICT:
Energy Aware Computation

Igor Neri - A pranzo con la Fisica
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Motivation

Energy-aware design, sometimes called energy-efficient design, is the design of a system to meet a given performance constraint with the minimum energy consumption.

- Critical in **battery-operated** devices.
- Critical in terms of **cost** (computer centers).
- Critical since energy is converted into **heat**.

How

- Algorithm: scheduling, power-down strategies
- Data management: memory-aware software optimization, routing protocol
- Architecture: instruction set selection, dynamic voltage and frequency scaling
- Virtualization: power saving of corporate data centers
- Circuit: device sizing, exploiting of transistor stacking to reduce leakage power

How

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Power down mechanism

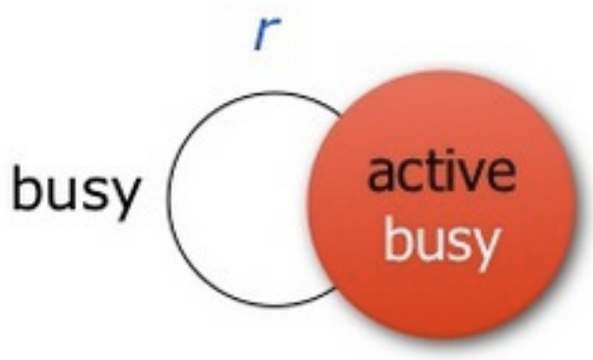
A system in idle state can be transitioned to **low power modes**

The goal is to develop transition schedules **minimizing energy consumption**

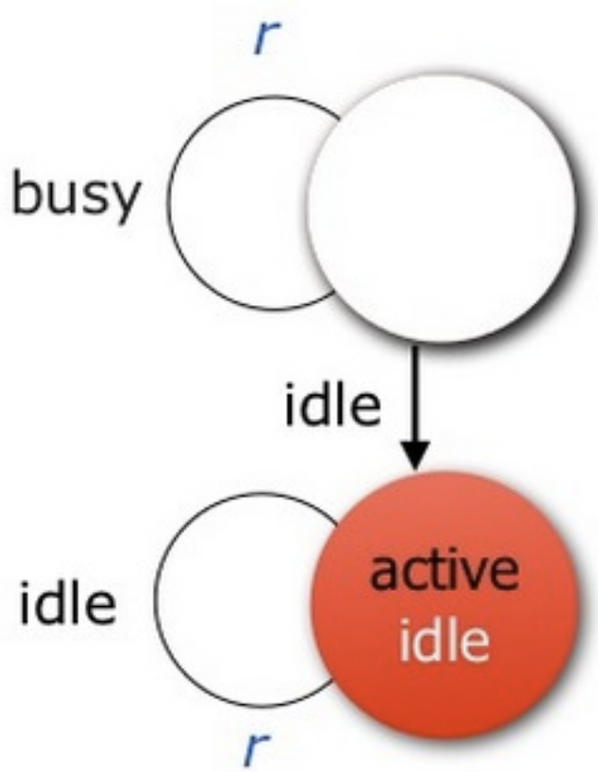
Power down mechanism:

- Two states system
- Multiple states system

Power down mechanism: two states system



Power down mechanism: two states system



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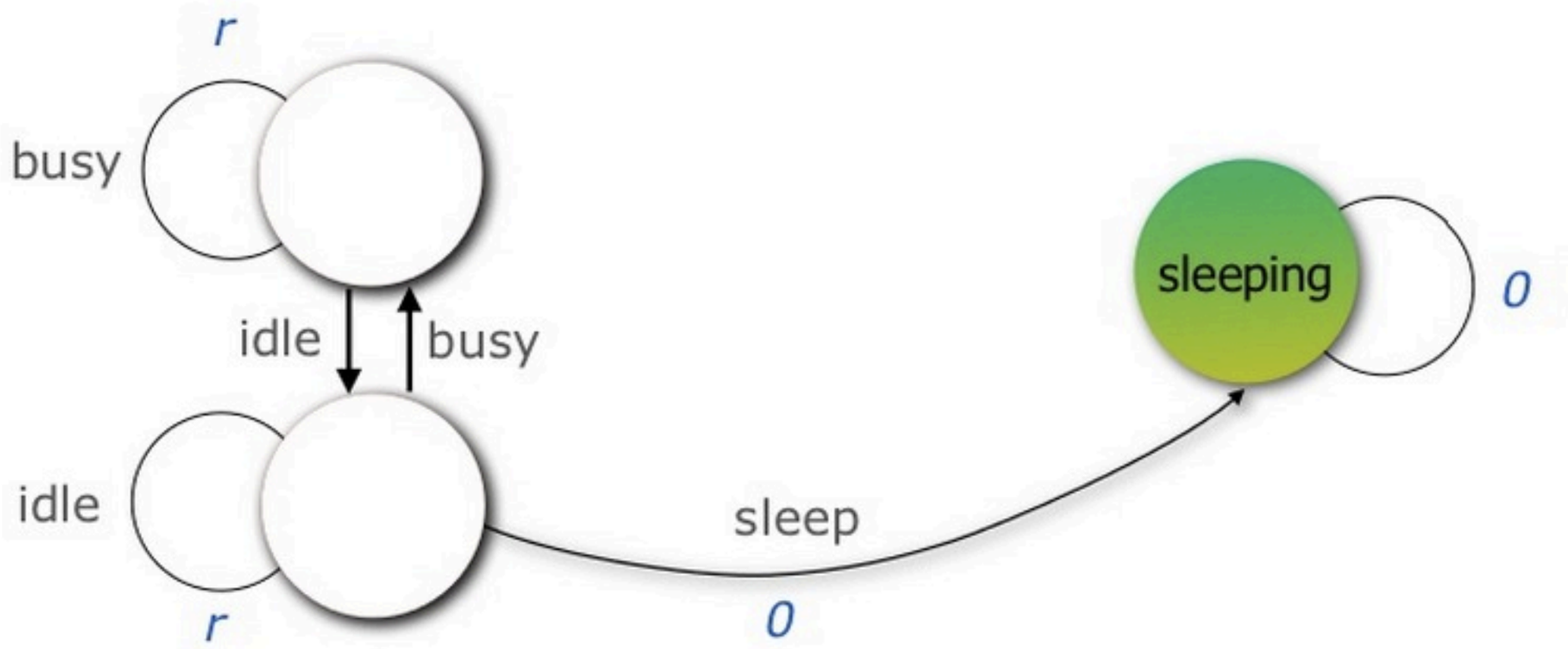
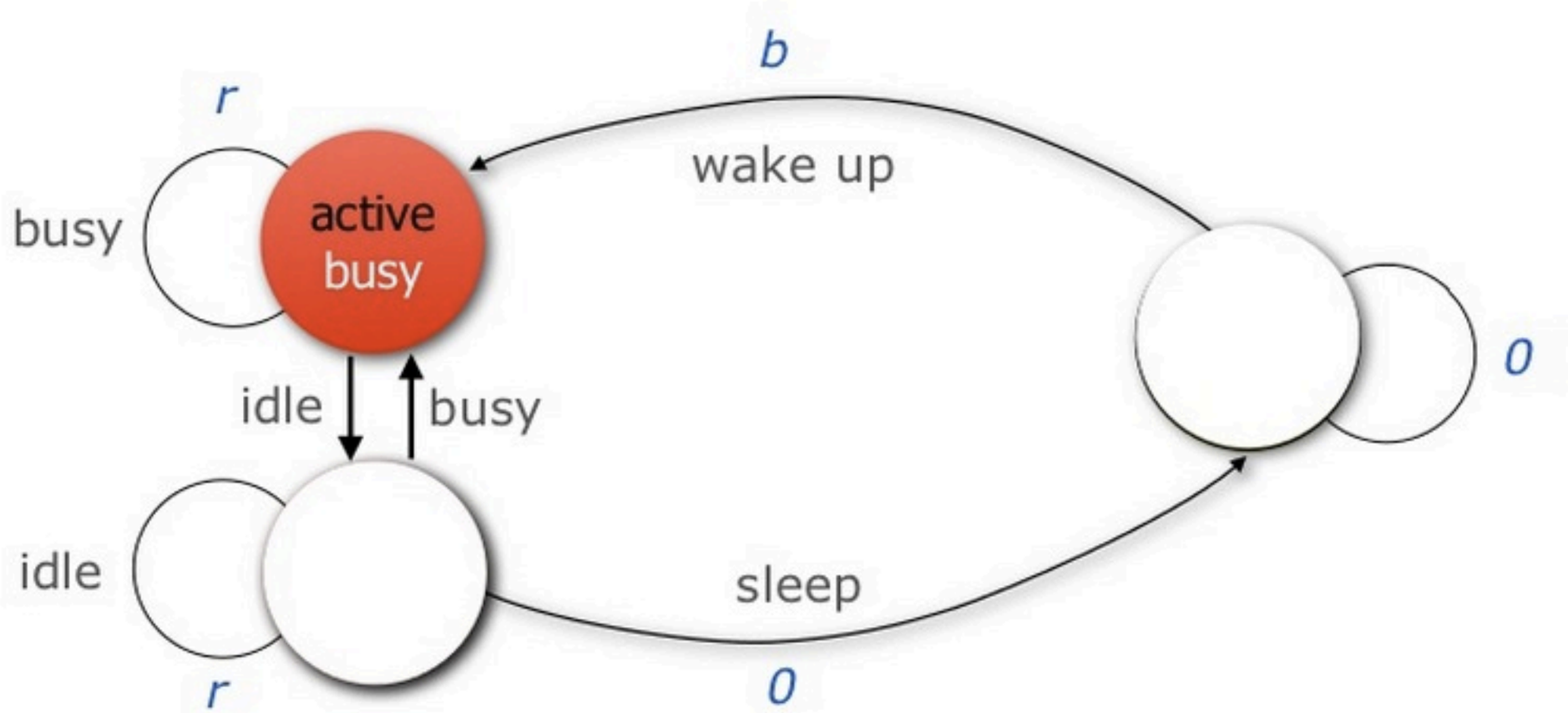
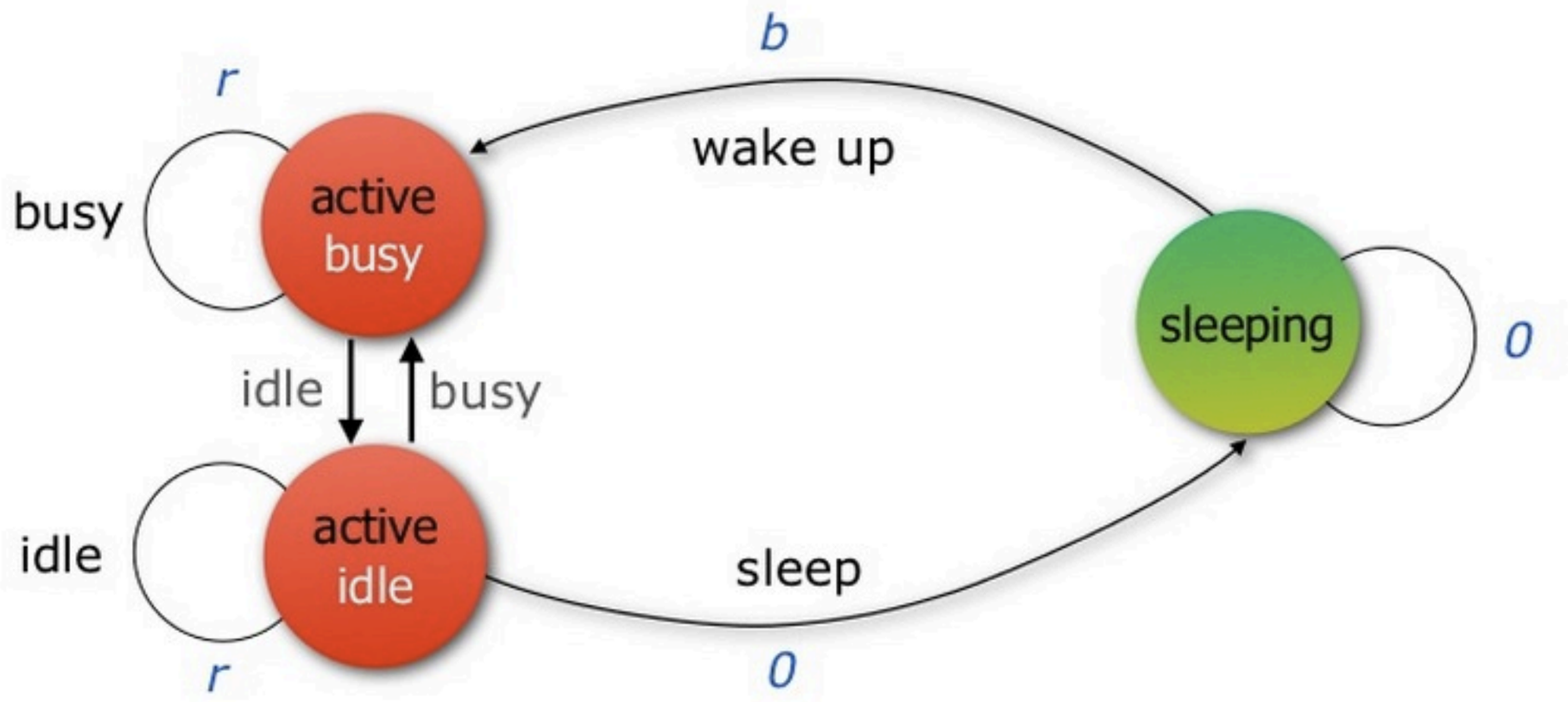


Power down mechanism: two states system

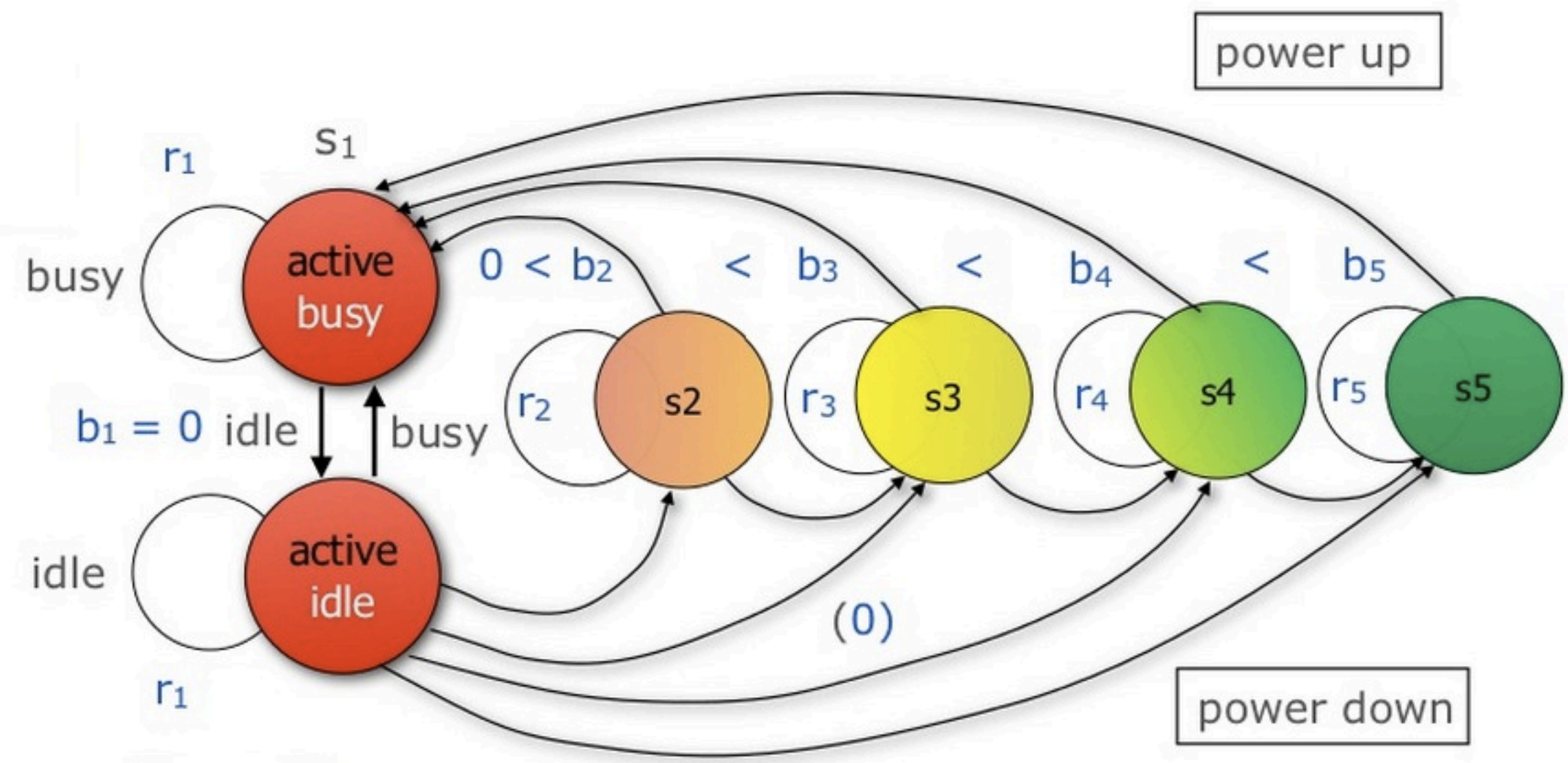


Power down mechanism: two states system

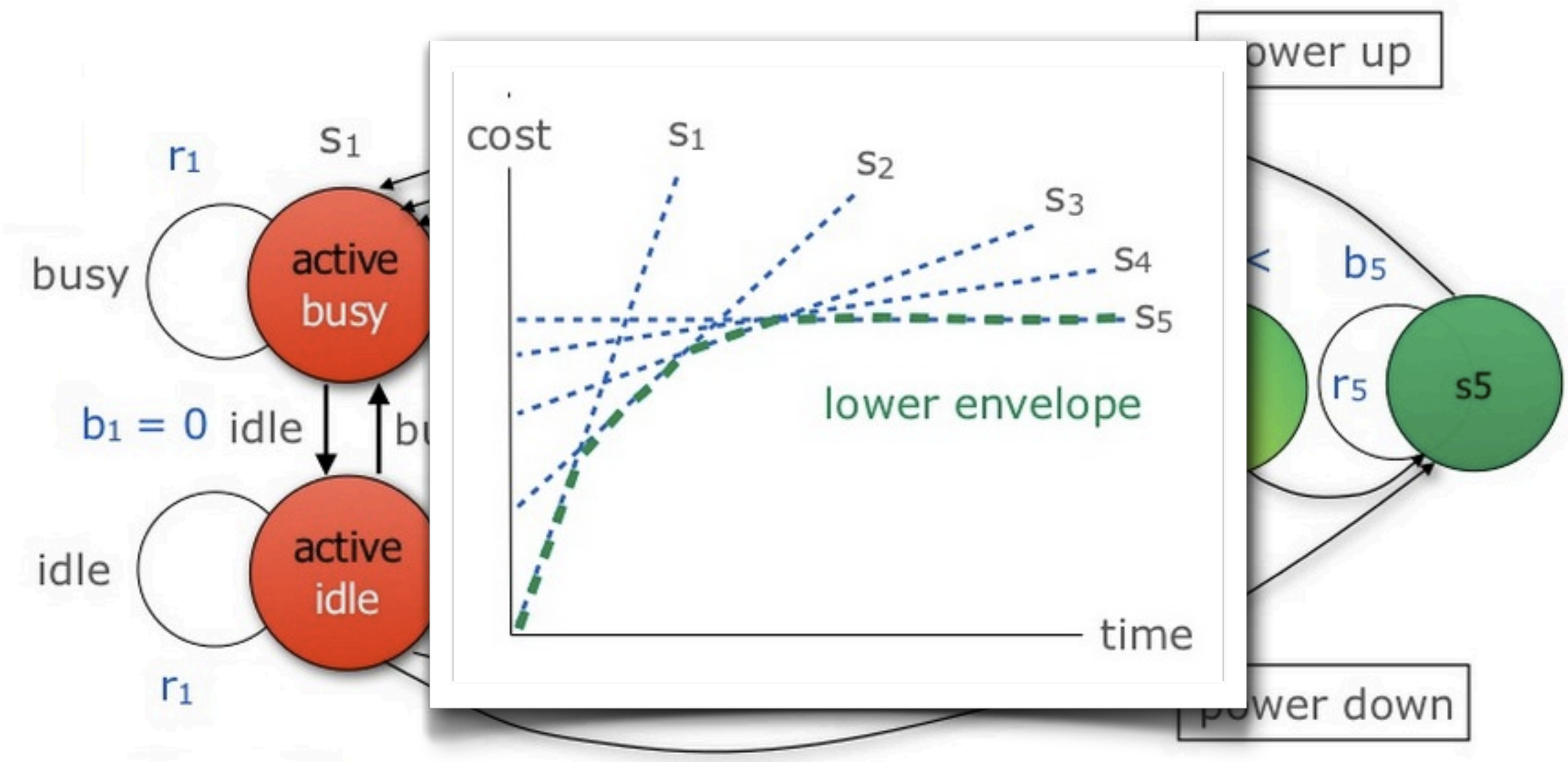


Problem: determine when to transition to the sleep state in order to minimize energy consumption.

Power down mechanism: multiple states system



Power down mechanism: multiple states system



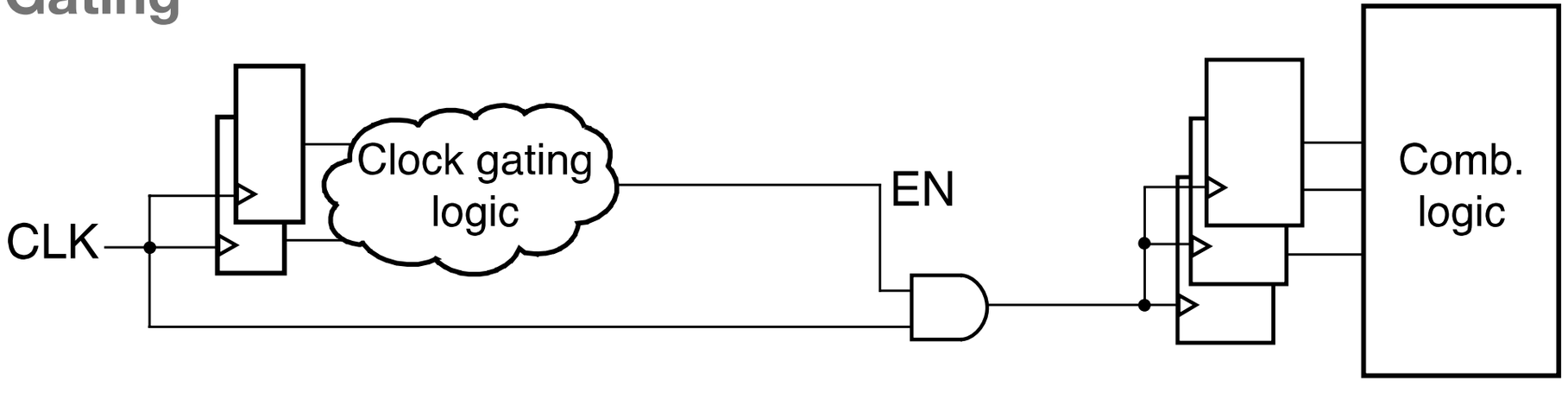
Circuits to reduce dynamic power

$$P_{sw} = \frac{1}{2}\alpha C_L V_{dd}^2 f$$

- **P_{sw}** average switch power consumption
- α probability of output switch
- **C_L** load capacitance
- f clock frequency
- **V_{dd}** operating voltage

Circuits to reduce dynamic power

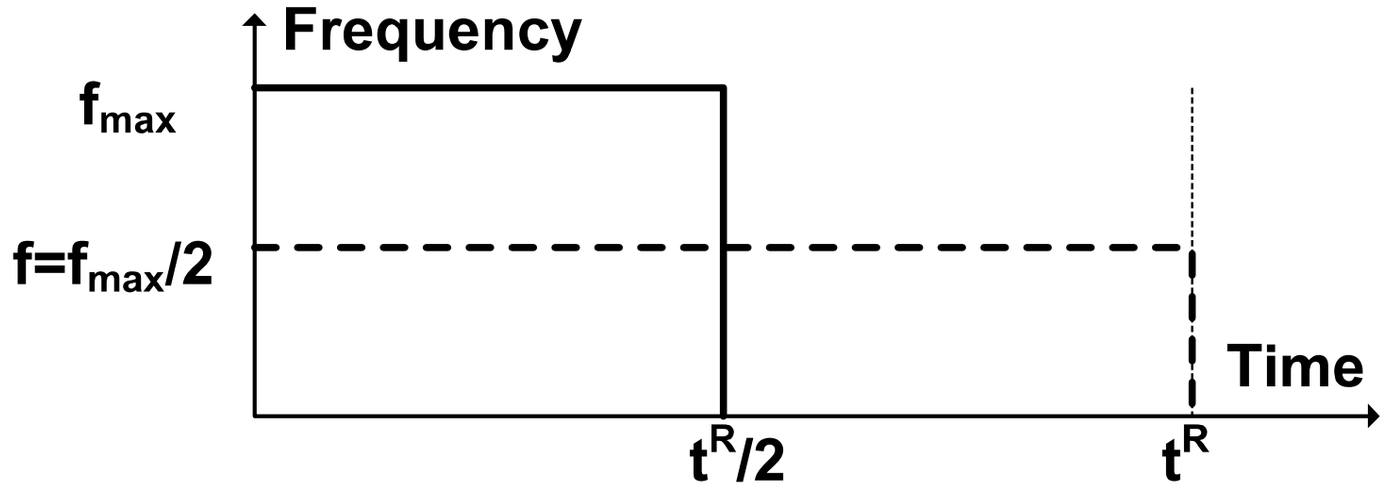
- **Clock Gating**



- **Dual V_{dd}**: V_{ddh} and V_{ddl}
  - V_{ddl} used for gates that not affect the overall circuit speed
  - Gate placement restricted (increase area and wire length)
  - Level conversion
  - Selection V_{ddl}:V_{ddh} is typically mandated by technology

Dynamic voltage and frequency scaling

$$f \propto \frac{(V_{\mathrm{dd}} - V_{\mathrm{th}})^{\alpha}}{V_{\mathrm{dd}}}$$



- V_{dd} operating voltage
- V_{th} threshold voltage
- α is a measure of velocity saturation ($1 \leq \alpha \leq 2$)

$$P_{\mathrm{dyn}} \propto f^{3}$$

Open problems & Hot topics

- Establishing metrics for assessing the energy efficiency of algorithms
- Estimation of the overhead caused by use of energy-aware algorithm
- Data aware computation
- Design of sub Landauer-limit logic gate and architecture
    - Design of noise tolerant algorithms

Thank you!