EMPLOYING TRANSPRECISION COMPUTING TECHNIQUES ON JPEG COMPRESSION SYSTEM

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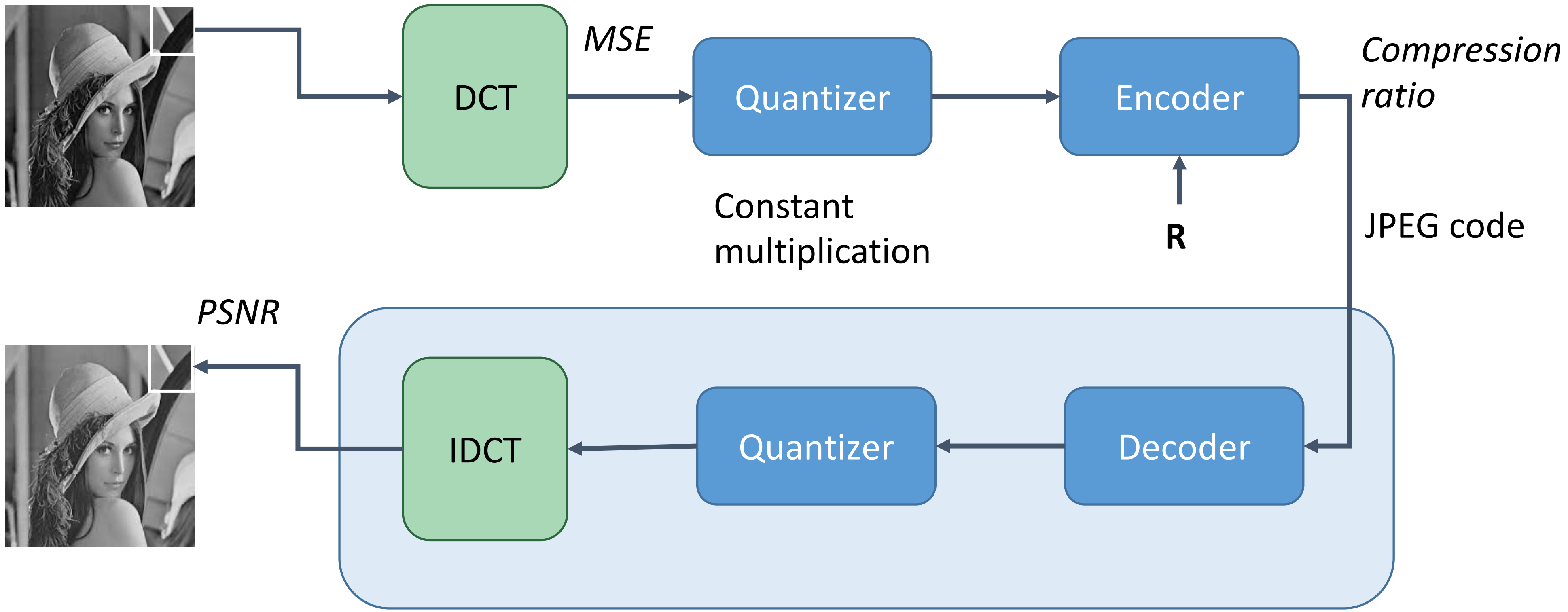
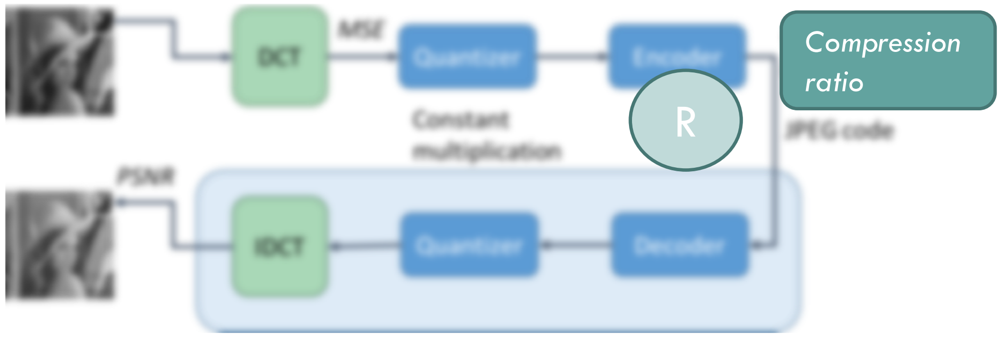
Architectures and Algorithms for Energy-Efficient IoT and HPC Applications

JPEG COMPRESSION SYSTEM

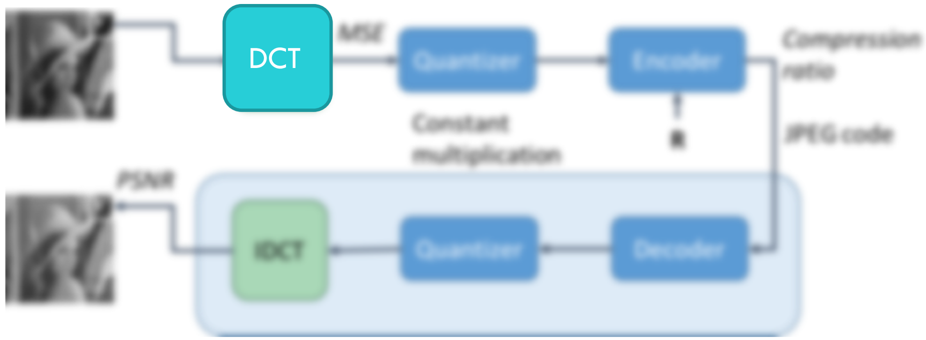


APPROXIMATION LEVELS

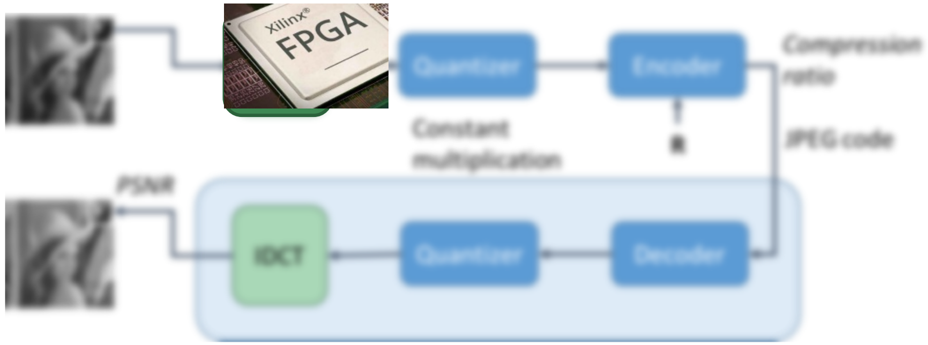
System level



Block level – Compiler level

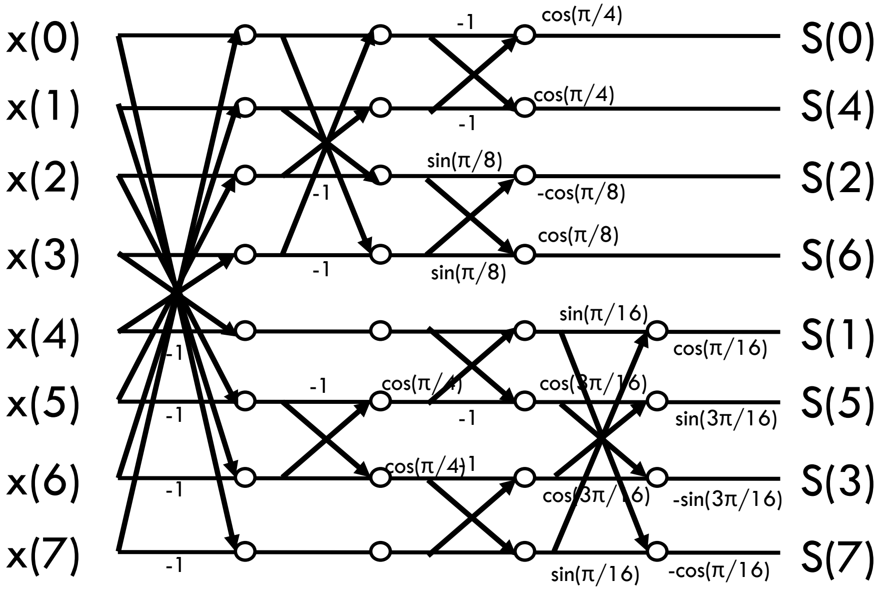


Circuit level

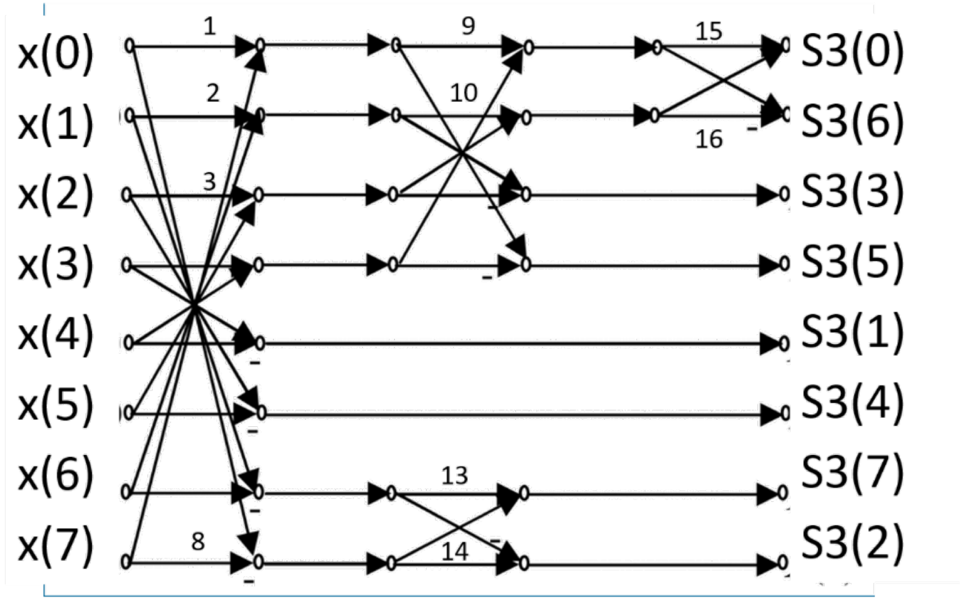


DISCRETE COSINE TRANSFORM

$$X_k = \sum_{n=0}^{N-1} x_n \cos\left[\frac{\pi}{N}\left(n+\frac{1}{2}\right)k\right] \qquad k = 0,\ldots,N-1$$



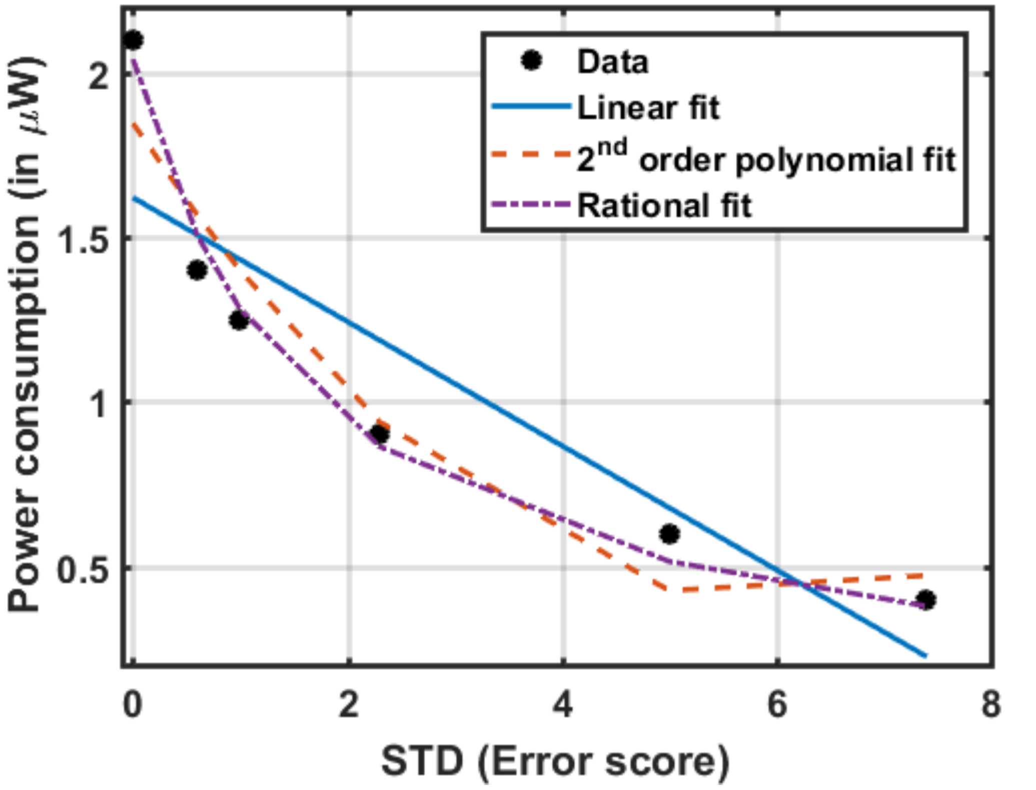
16 Multiplications and
36 Additions



16 Additions

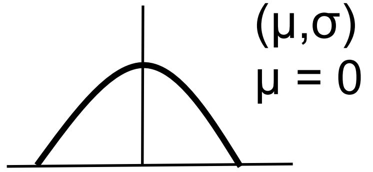
FIND OPTIMUM ADDERS

Minimize: $\sum_{i=1}^{N} P(\hat{X}_i)$



Total power consumption of arithmetic computing units will be minimized.

$X = [X_1 \ldots X_{16}]$ → Error of adder



Power consumption of an adder:

$P\ (X_i) = a \times X_i + b$

FIND OPTIMUM ADDERS

Minimize: $\sum_{i=1}^{N} P(\hat{X}_i)$

Subject to:

$$B\hat{X} \leq b$$
$$\hat{X} \geq LB$$
$$\hat{X} \leq UB$$
$$\hat{X}_i \in \mathbb{R} \,,\ 1 \leq i \leq N$$

The desired performance will be maintained.

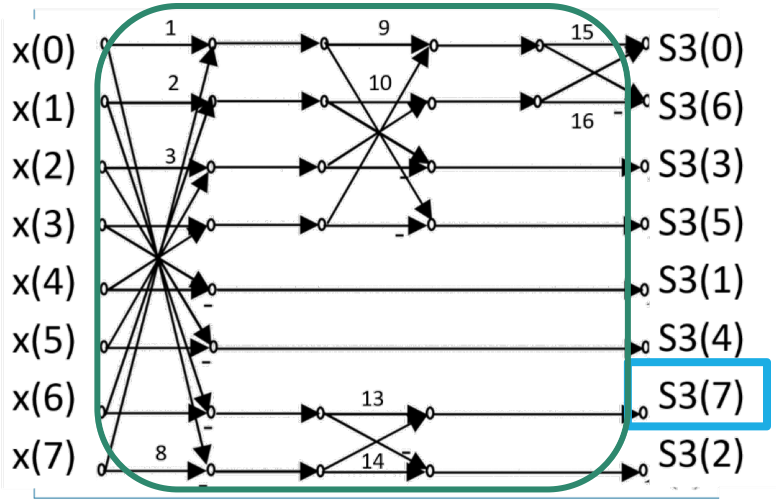
JPEG Compression → PSNR

b → MSE

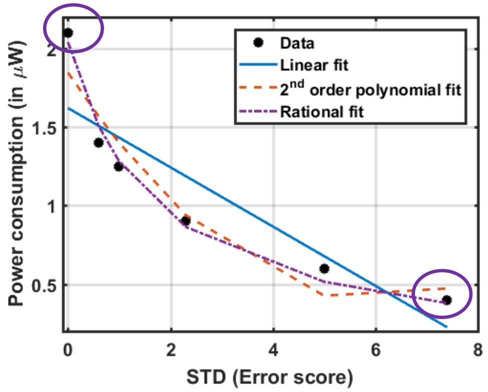
B → Connections within the blocks

UB → 7.2

LB → 0



Least important component



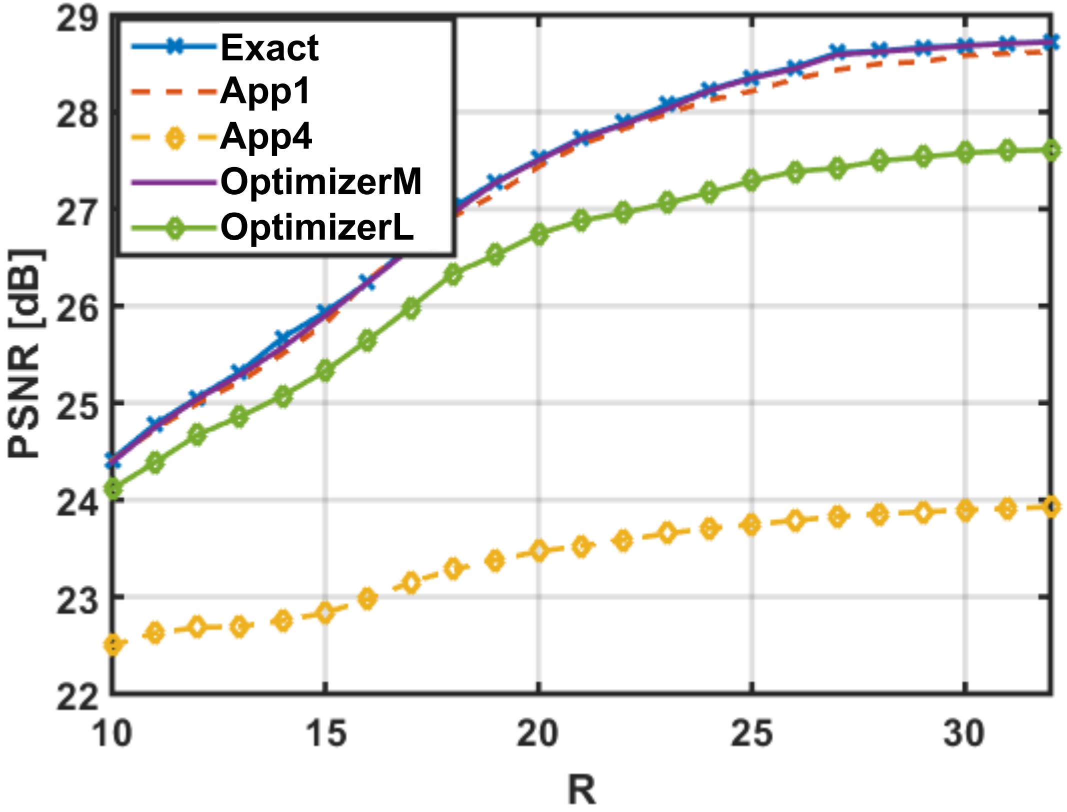
USE CASES

- Low PSNR requirement: Energy saving is very important, i.e. compressed image is transmitted from a battery-powered node in an IoT application.
  - All identical approximate adders.
  - Optimizer is used: 2dB PSNR loss is allowed.
- Medium PSNR requirement: Energy saving is important, i.e. compressed image is transmitted for entertainment in a social media application.
  - All identical approximate adders.
  - Optimizer is used: 0.5dB PSNR loss is allowed.
- High PSNR requirement: Baseline.
  - Exact adders are used.

RESULTS 1/2

Use-Case	Adders	Power [mW]	Power Saving [%]	PSNR [dB]	PSNR loss [%]
Low PSNR	Identical app4	0.6575	48.0939	23.1716	19.5125
	OptimizerL	0.9475	25.1211	27.9481	4.1274
Medium PSNR	Identical app1	1.1650	7.8969	28.8644	0.9841
	OptimizerM	1.1175	11.6688	28.2875	2.9631
High PSNR	Exact	1.3671	-	29.1513	-

RESULTS 2/2



App1

App4

OptimizerM

OptimizerL

CONCLUSION

- 2 of 3 levels of approximation are used: block (compiler) level and circuit level.
- The adders are not optimized for FPGA implementation. Results can be improved by designing the circuits for the target platform.
- Algorithm level approximation (compression ratio) gives the best saving, as expected.
- Objective function of the optimizer can be linear or non-linear; non-linear objective function did not change the adder combination for this problem.

Thank you.

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